



Q57H-AM

V : 1.0

SCHEMATICS TABLE:


Page	Index
1	COVER PAGE
2	Block Diagram
3	CPU-MISC&FDI Link
4	CPU DMI&PEG
5	CPU DDR3-A
6	CPU DDR3-B
7	CPU CFG
8	CPU Power(VCCP,V_AXG,VTT)
9	CPU GND&RSVD
10	PCI-E 16X
11	CONN DDR3 CH A DIMM2
12	CONN DDR3 CH A DIMM1
13	CONN DDR3 CH B DIMM4
14	CONN DDR3 CH B DIMM3
15	PCH USB&PCIE&DMI
16	PCH SATA,HOST,CLINK,PCI
17	PCH GPIO,AUDIO,LPC,SPI,BAT
18	PCH NVRAM
19	PCH FDLINK&SPI ROM&TPM
20	PCH PWR RAILS,Decoupling
21	PCH GND Pins
22	PCH Video and DDSP
23	PCH CLOCKS,Straps

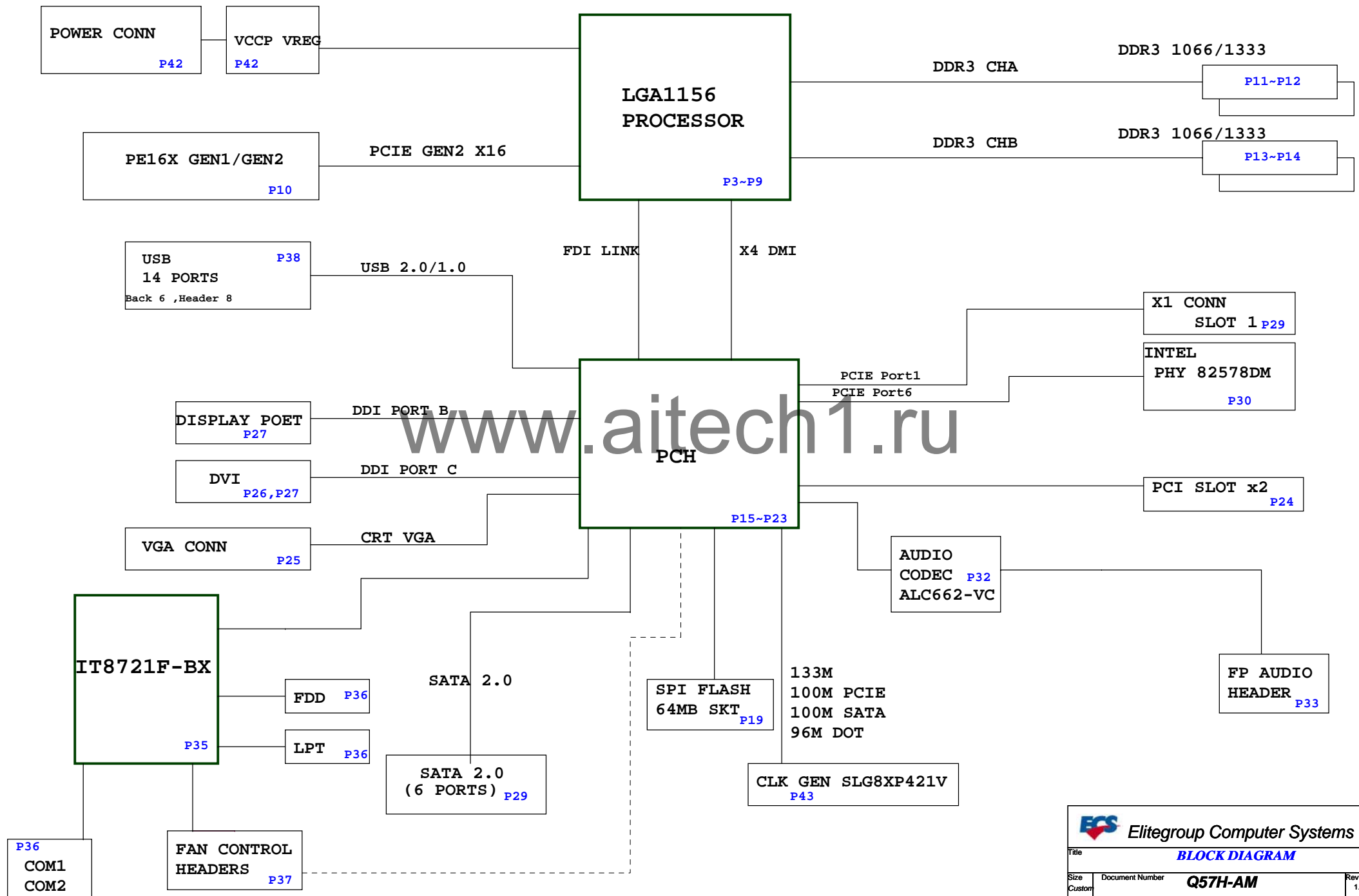
Page	Index
24	PCI
25	VGA Connector
26	DVI-D Interface(Shift)
27	DVI-D&DISPLAY CONN
28	Primary&PCH XDP
29	SATA&PCI-EX1
30	Hanksville Lan(82578DM)
31	AMT6.0
32	AUDIO ALC662-VC
33	Audio Connector(PANEL)
34	EUP LOT6
35	IT8721F-BX
36	COM,KBMS,FDD,LPT
37	PANEL&Smart Fan
38	USB Header&Port
39	DC-DC3 CPU_VTT,5VDUAL
40	DC-DC2 V_AXG,V_1P05_ME
41	DC-DC4 PCH Core,VDIMM,V_1P8
42	DC-DC Vcore
43	CLK GEN SLG8XP421V
44	POWER DELIVERY
45	PWRGD AND RST Tree
46	Clock Map

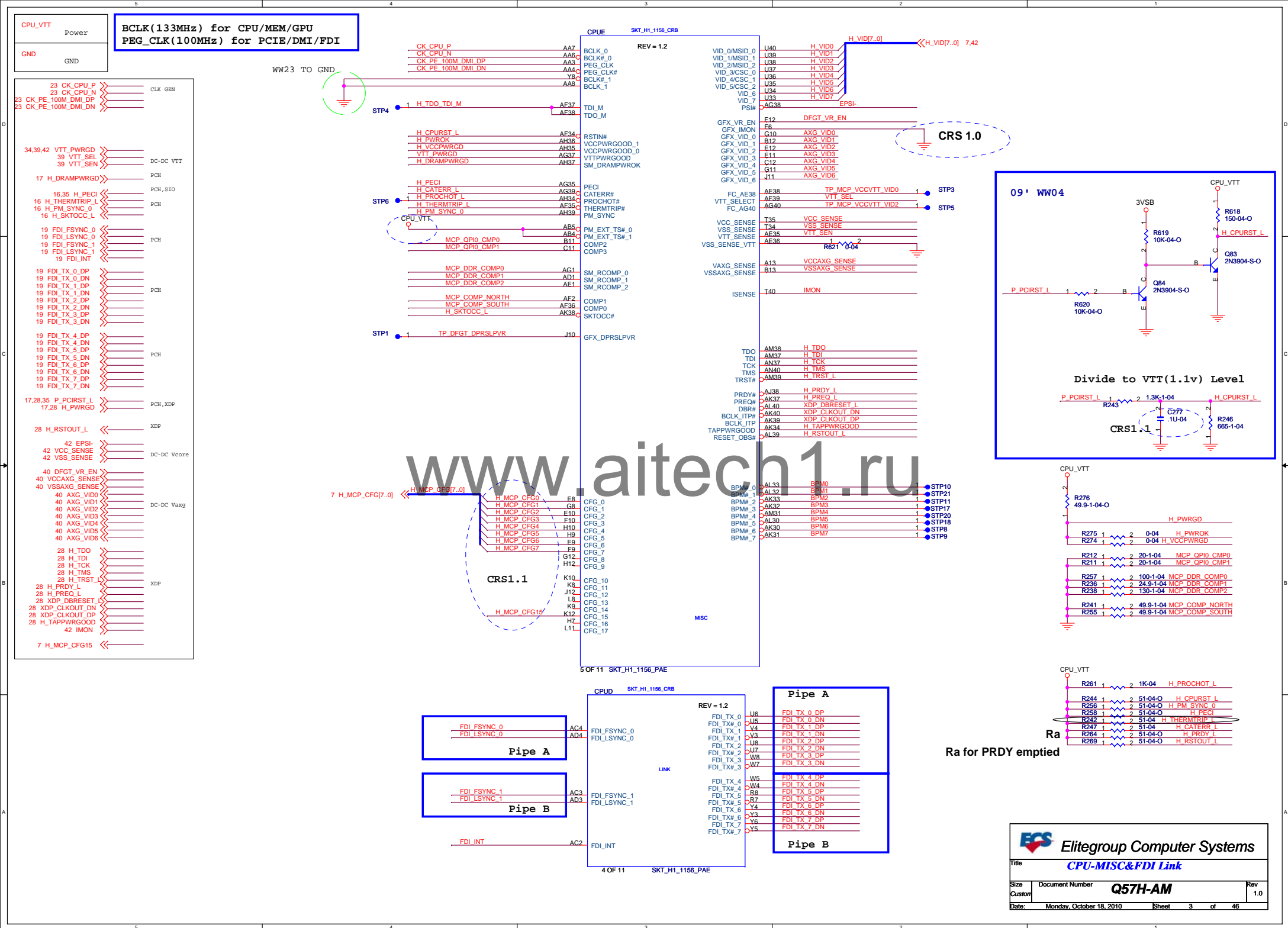
REVISION HISTORY:

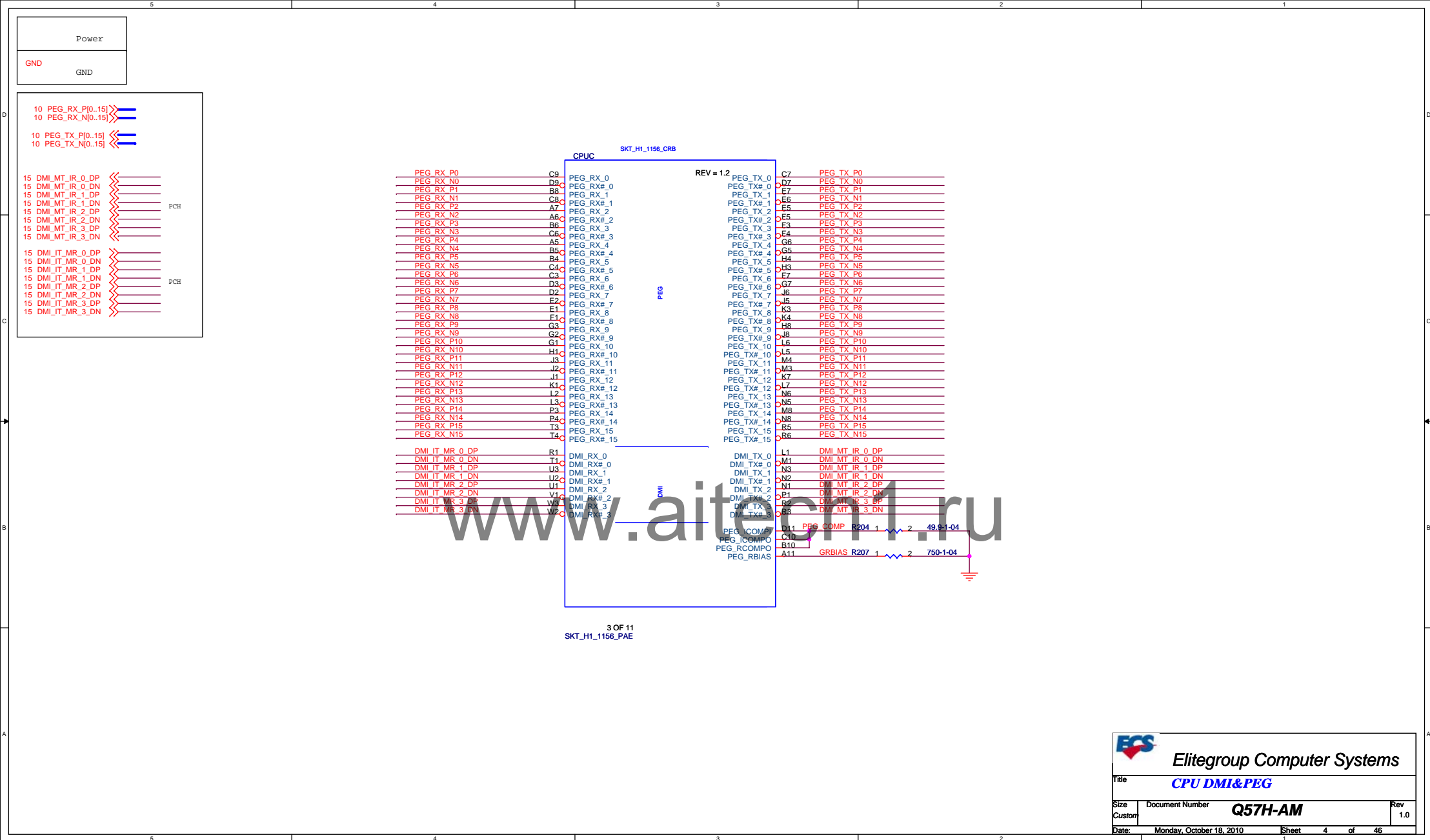
Rev	Date	Notes
-----	------	-------

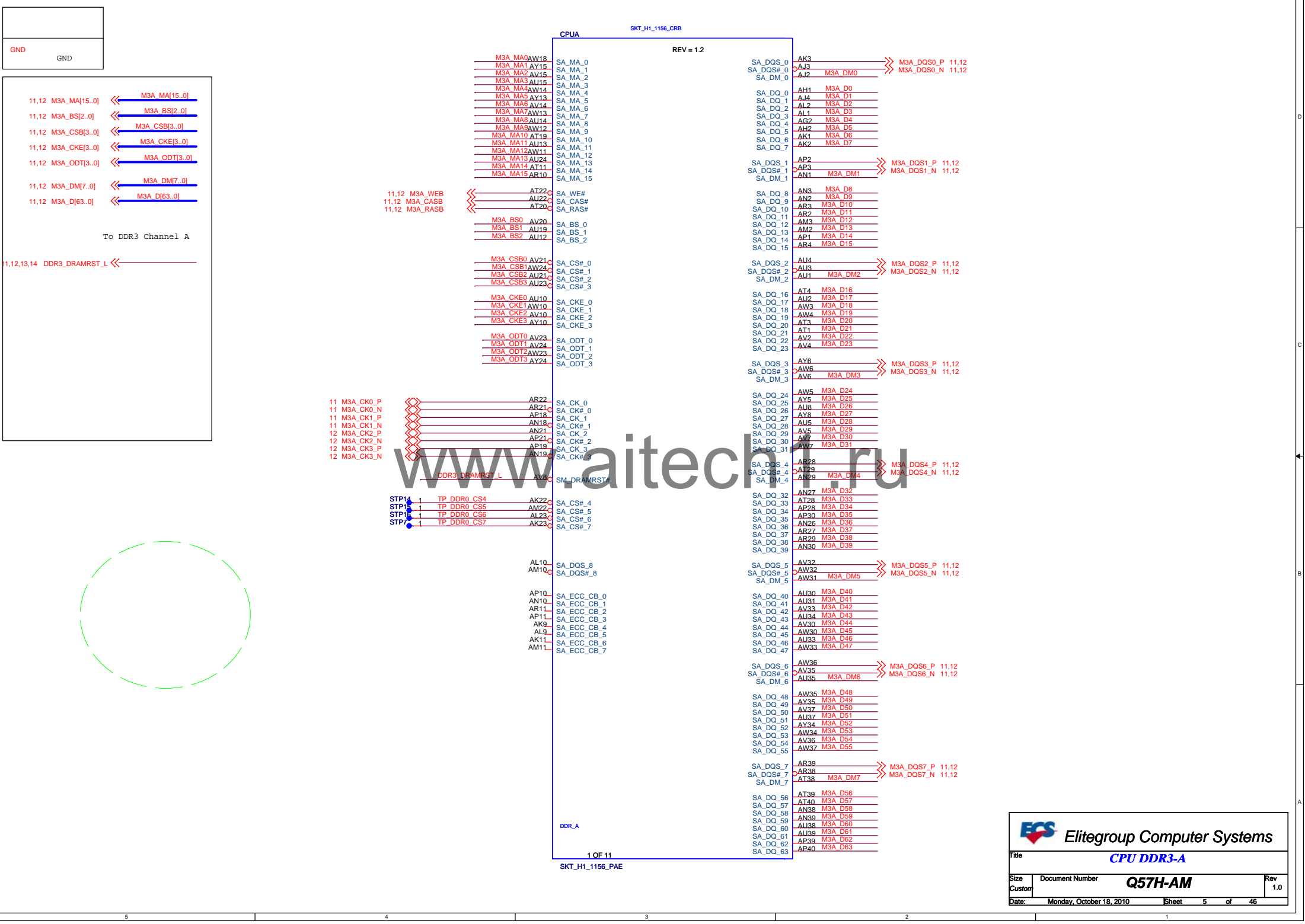
@ ECS
CONFIDENTIAL @

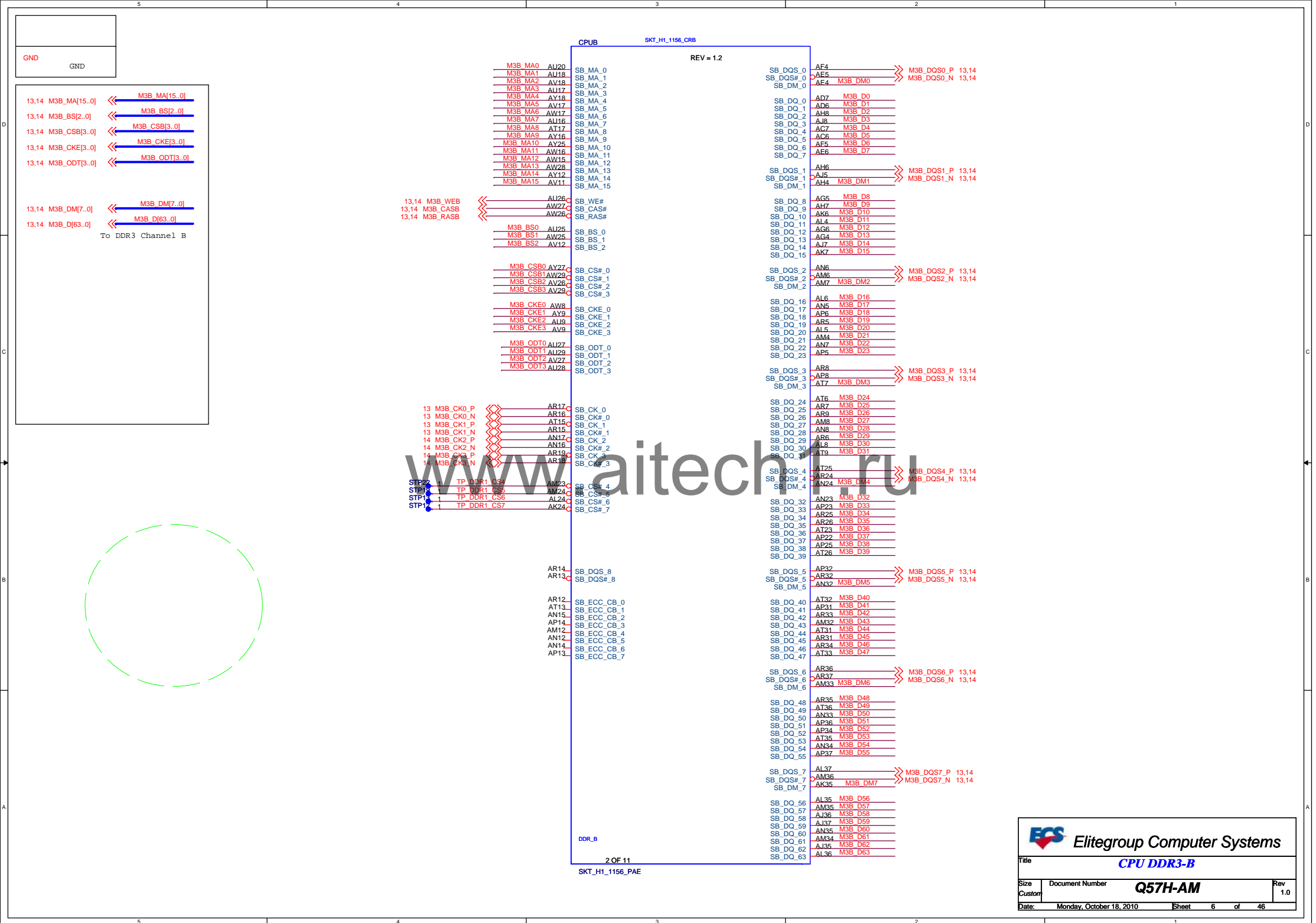
 Elitegroup Computer Systems	
Title Cover Page	
Size Custom	Document Number Q57H-AM Rev 1.0
Date: Monday, October 18, 2010	Sheet 1 of 46



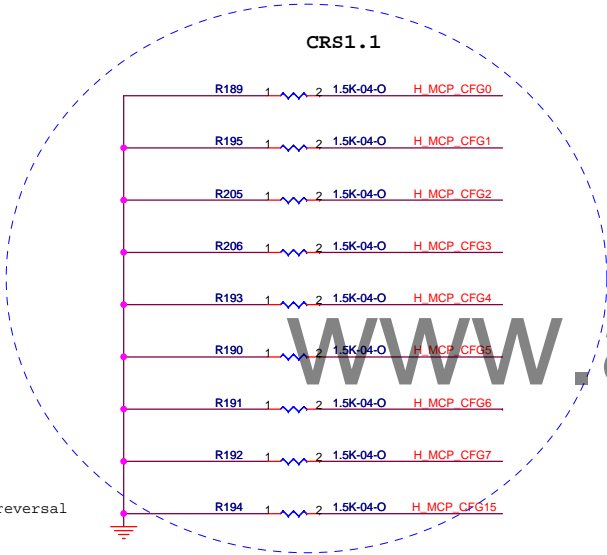
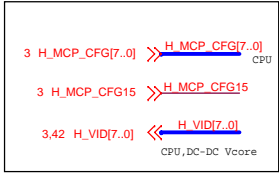






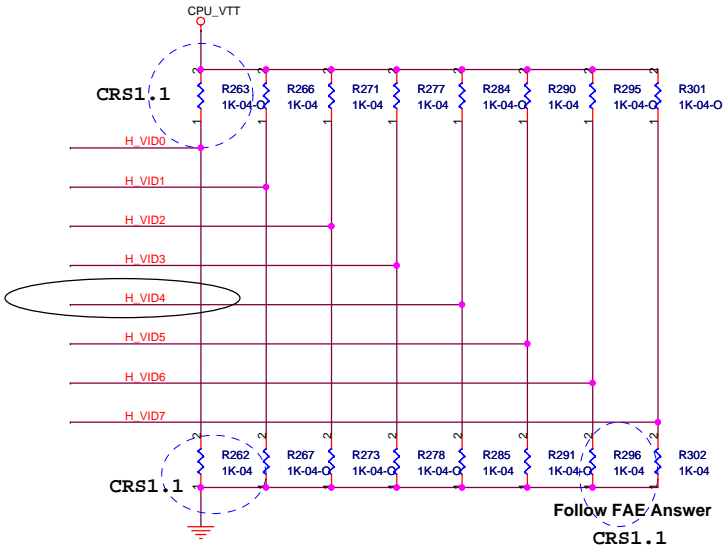


CPU_VTT	Power
GND	GND



CFG(1:0)
Desktop
11 PCIe16X
10 PCIe18X
CFG2,4,5,6,7~17
Reserved configuration land
CFG3
Havendale PCIe static Lan Numbering reversal

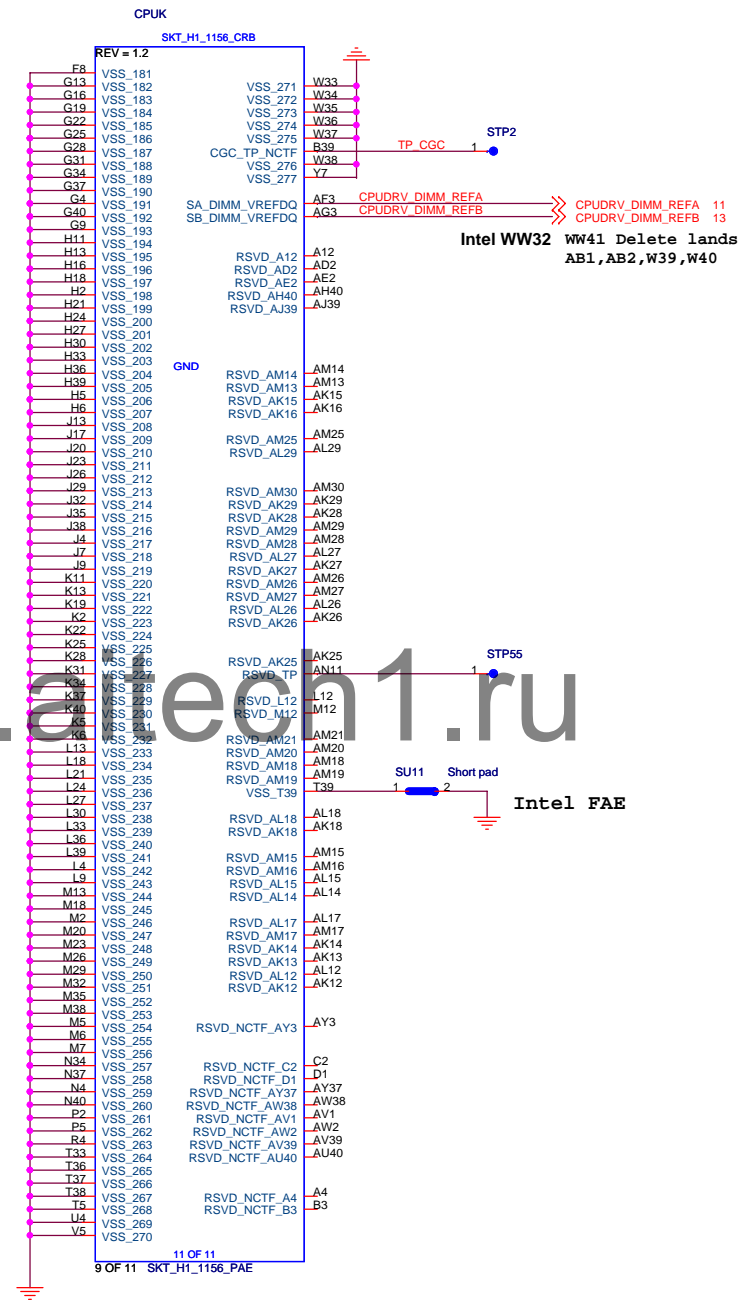
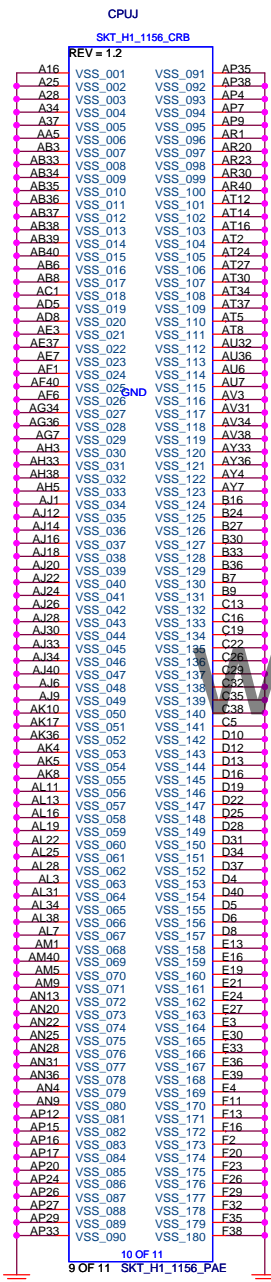
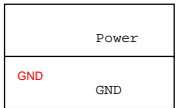
CFG	Havendale	Lynnfield			
0	REVERSED	1	11=1*16X	0	10=2*8X
1	REVERSED	1		1	
2	REVERSED			REVERSED	
3	Static Lane Number Reversal			REVERSED	
4	REVERSED			REVERSED	
6	REVERSED				
7	REVERSED				
15	REVERSED				
0,1,2,3,4,5 ALL HAVE INTERNAL PULL-UPS					

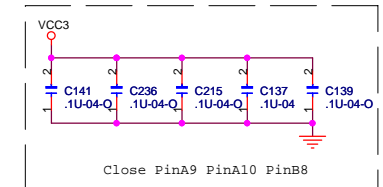


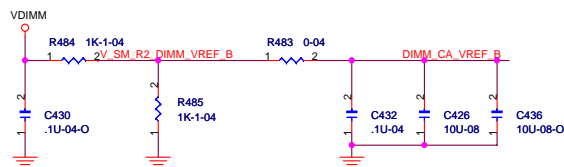
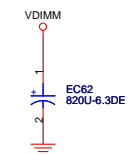
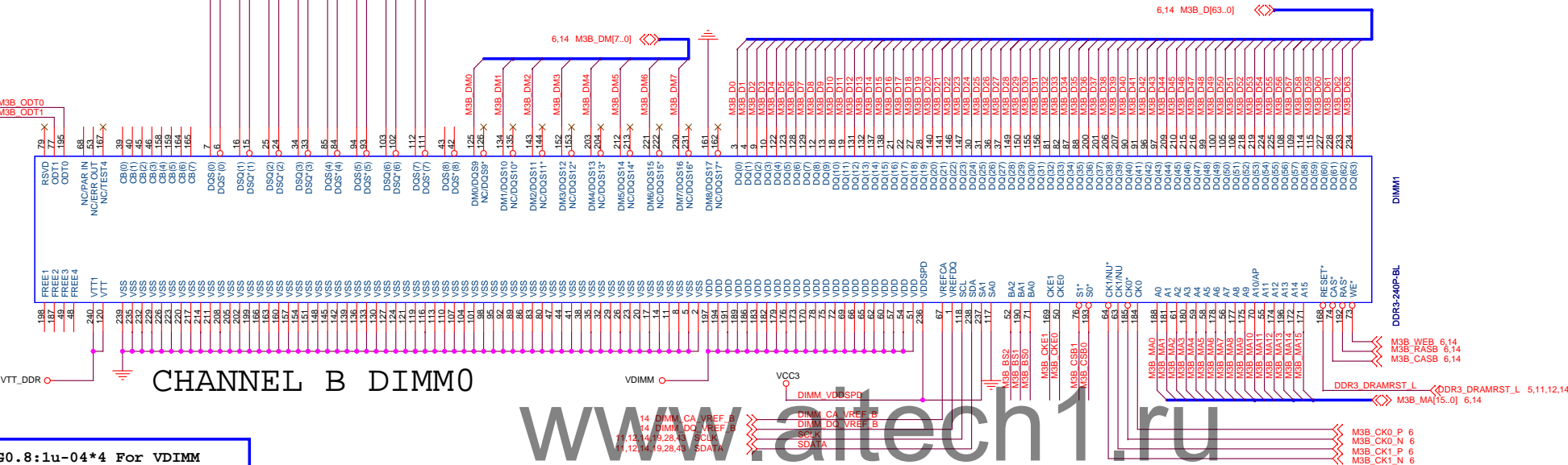
POWER ON CONFIGURATION (POC)TABLE

	FUNCTION	Setting	Havendale	Lynnfield
VID0	MIS0	0	Support	Support
VID1	MIS1	1		
VID2	MIS2	1		
VID3	IMON CONFIG CSC0	1	Icc(MAX)=120A	Icc(MAX)=120A
VID4	IMON CONFIG CSC1	0		
VID5	IMON CONFIG CSC2	1		
VID6	RESERVED	0		
VID7	VID SELECT	0		
PSI#	RESERVED	LOW		

*MSID(2:0)
110 Lynnfield and Havendale support
*CSC(0:2)
Iout Gain and POC setting
100 ICC(max) 80A~100A
101 ICC(max) 100A~120A
110 ICC(max) 120A~140A







6,13 M3B_DQS7_N
6,13 M3B_DQS7_P
6,13 M3B_DQS6_N
6,13 M3B_DQS6_P
6,13 M3B_DQS5_N
6,13 M3B_DQS5_P
6,13 M3B_DQS4_N
6,13 M3B_DQS4_P
6,13 M3B_DQS3_N
6,13 M3B_DQS3_P
6,13 M3B_DQS2_N
6,13 M3B_DQS2_P
6,13 M3B_DQS1_N
6,13 M3B_DQS1_P
6,13 M3B_DQS0_N
6,13 M3B_DQS0_P

M3B_ODT2
M3B_ODT3

6,13 M3B_DM[7..0]

6,13 M3B_D[63..0]

CHANNEL B DIMM1

13 DIMM_CA_VREF_B
13 DIMM_DQ_VREF_B
11,12,13,19,28,43 SCLK
11,12,13,19,28,43 SDATA

DIMM CA_VREF_B
DIMM DQ_VREF_B
SCLK
SDATA

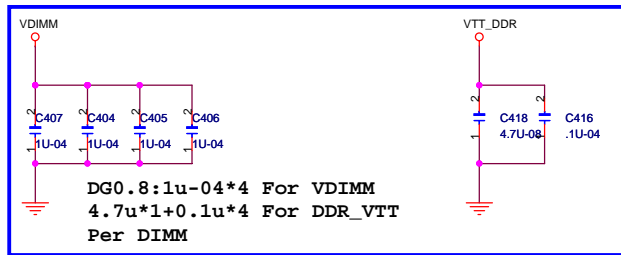
DDR3_DRAMRST_L 5,11,12,13

M3B_CK2_P 6
M3B_CK2_N 6
M3B_CK3_P 6
M3B_CK3_N 6

M3B_WEB 6,13
M3B_RASB 6,13
M3B_CASB 6,13

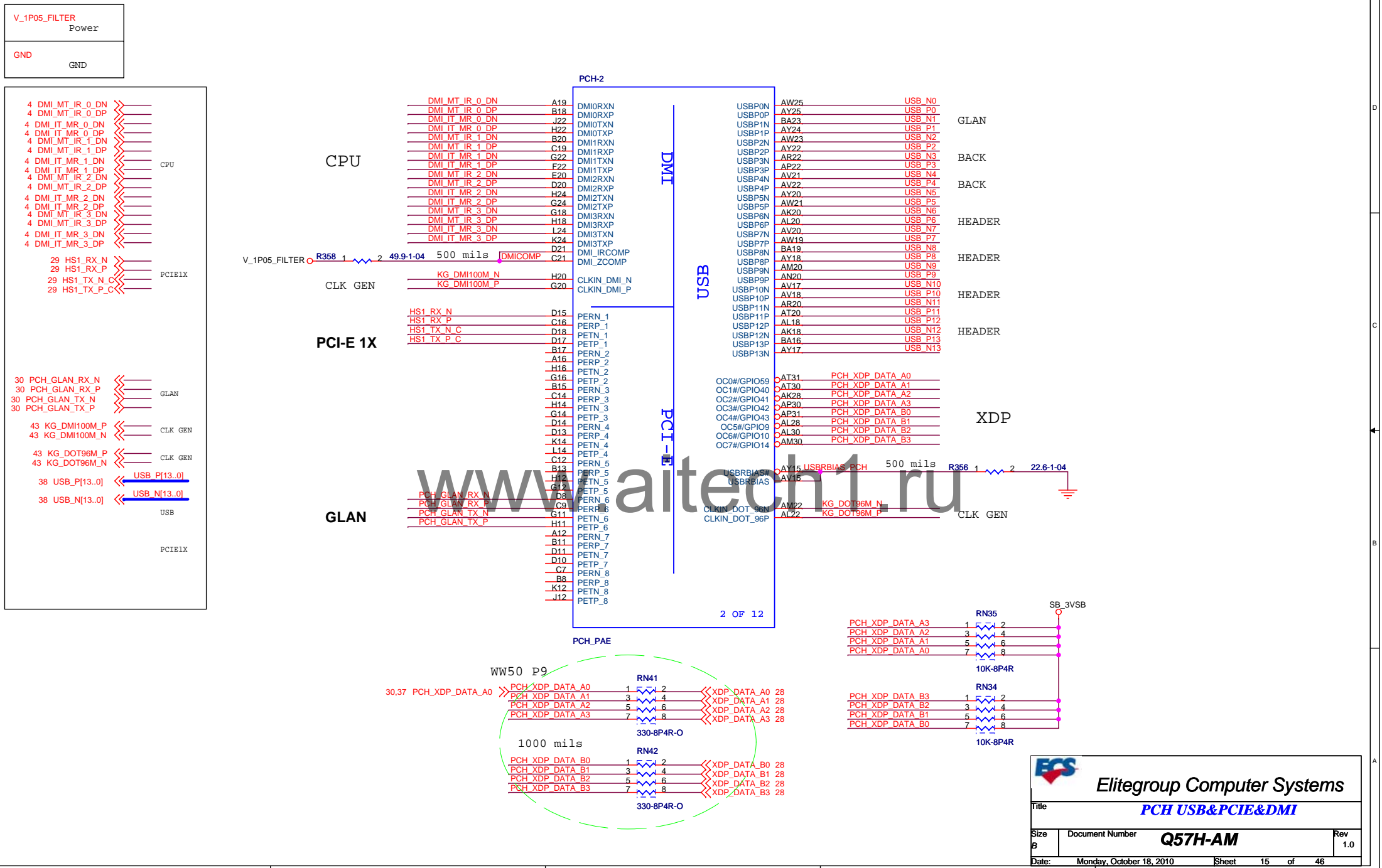
DDR3-240P-GR

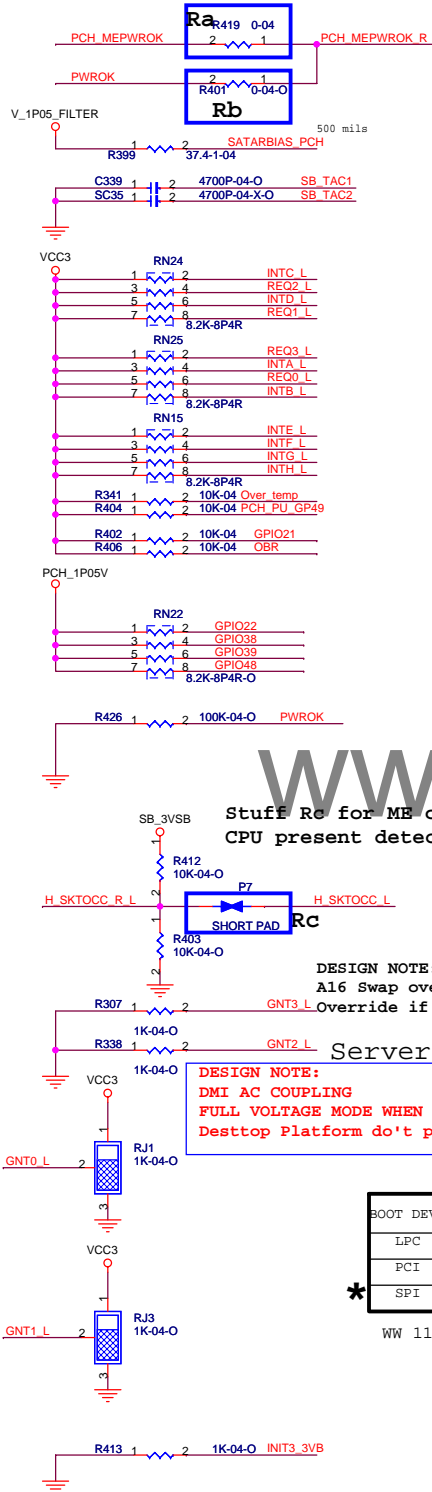
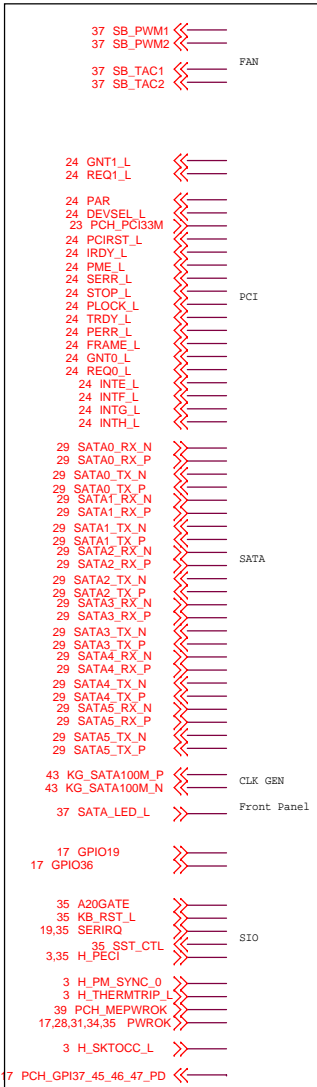
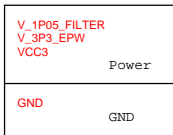
DIMM3



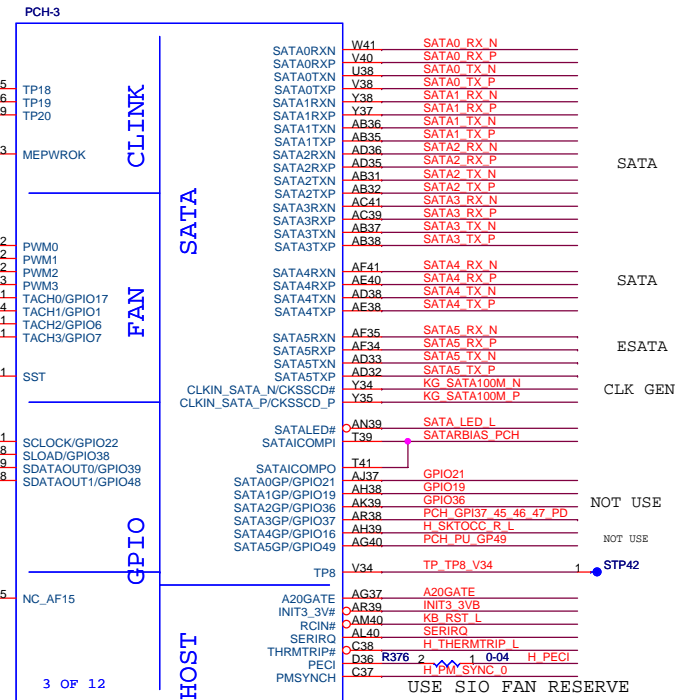
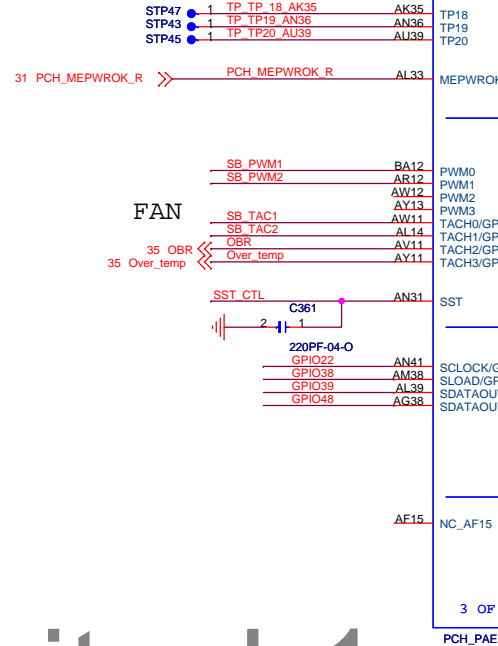
DDR_VTT	Power
VDIMM	
DIMM_VDDSPD	
GND	GND

6,13 M3B_MA[15..0]
6,13 M3B_ODT[3..0]
6,13 M3B_CSB[3..0]
6,13 M3B_CKE[3..0]
6,13 M3B_BS[2..0]





ME_PWROK		
AMT		Ra
Non-AMT		Rb



www.aitech1.ru

Stuff R# for ME on CPU present detection

DESIGN NOTE:
A16 Swap override BIOS
Override if sampled low

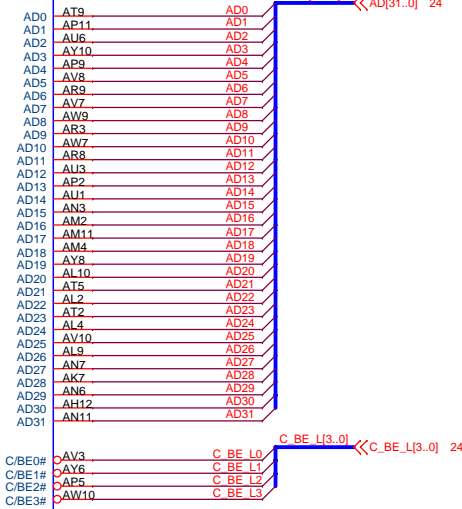
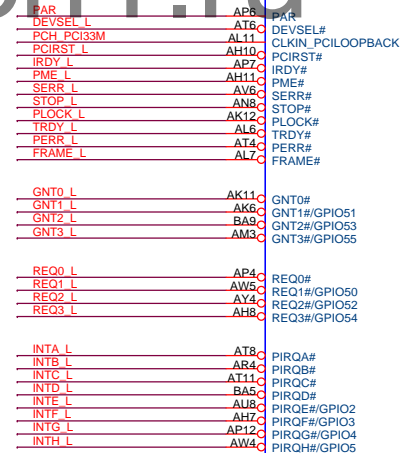
Server Only
DESIGN NOTE:
DMI AC COUPLING
FULL VOLTAGE MODE WHEN SAMPLED LOW
Desktop Platform do't pull low

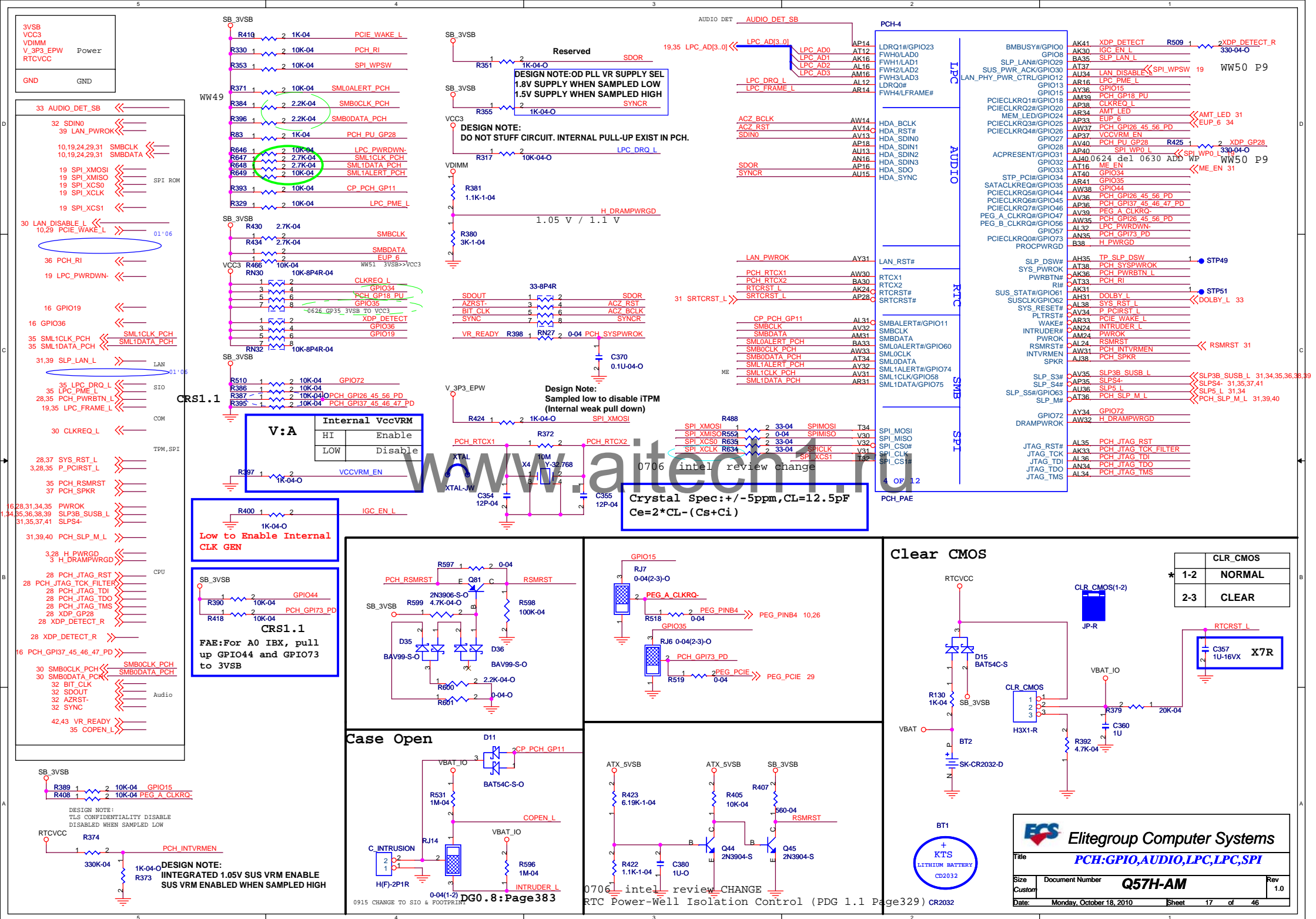
BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	1	0
SPI	1	1

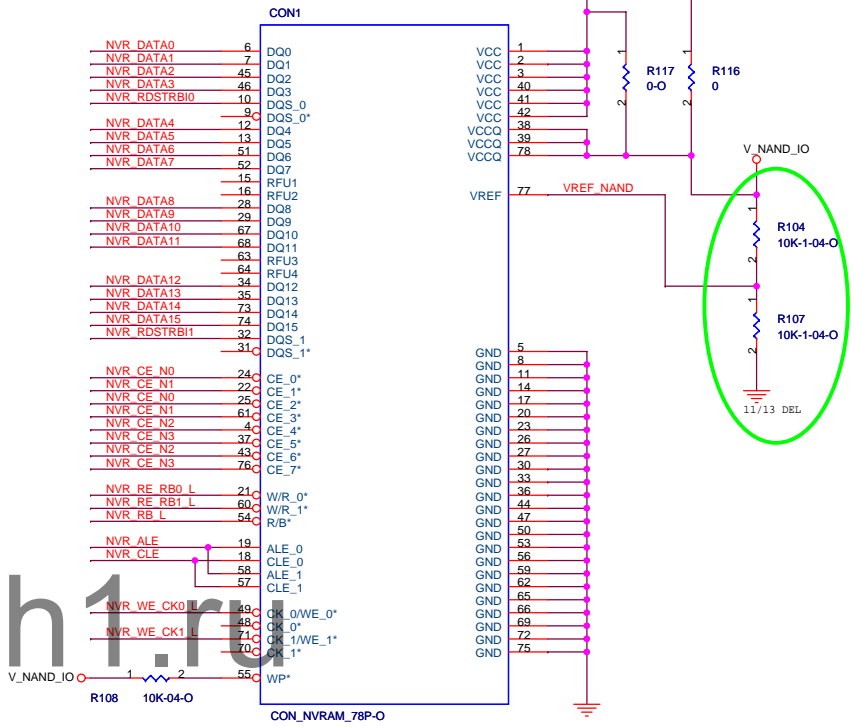
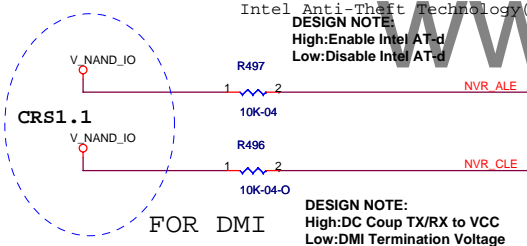
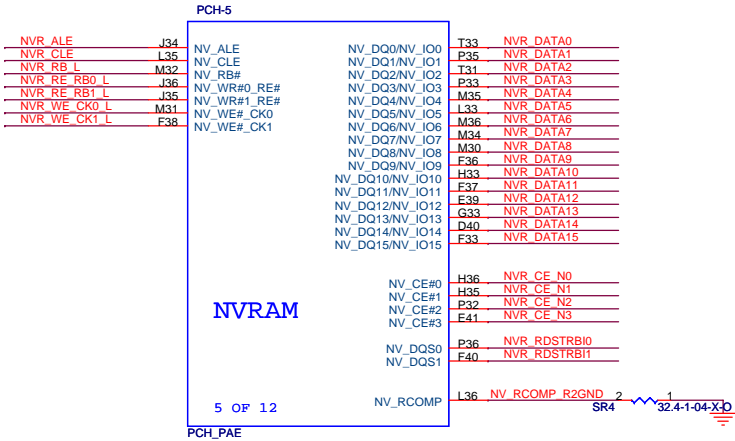
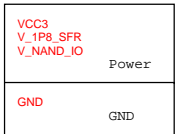
WW 11 PCI CHANGE TO 10

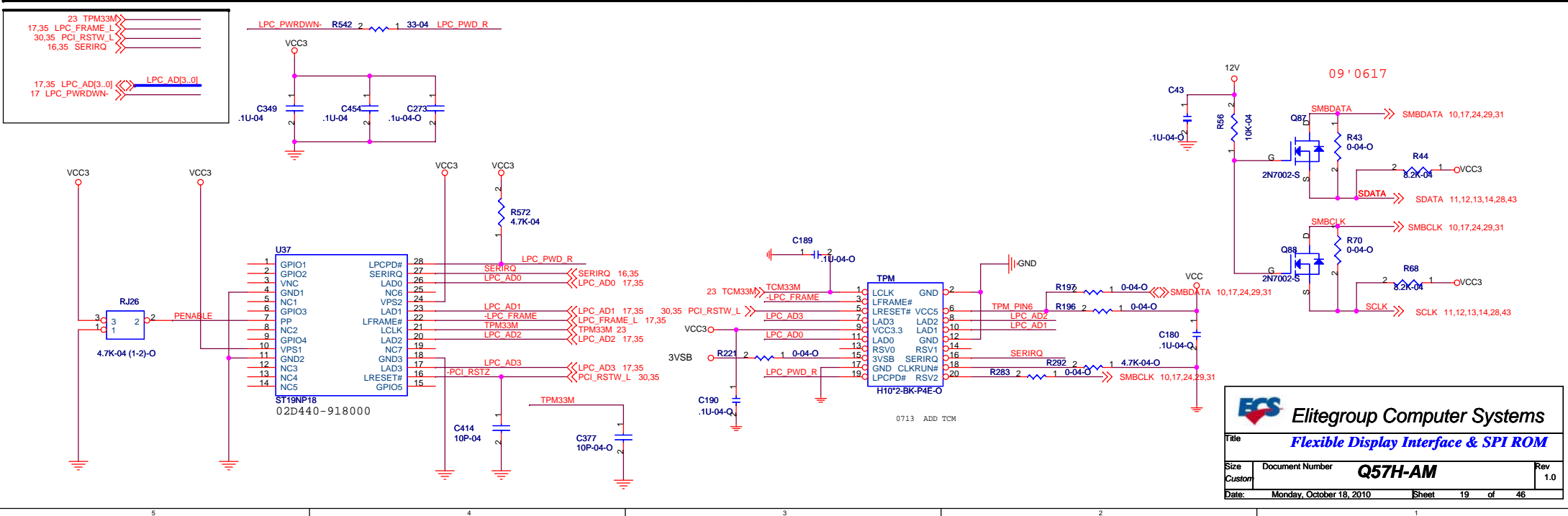
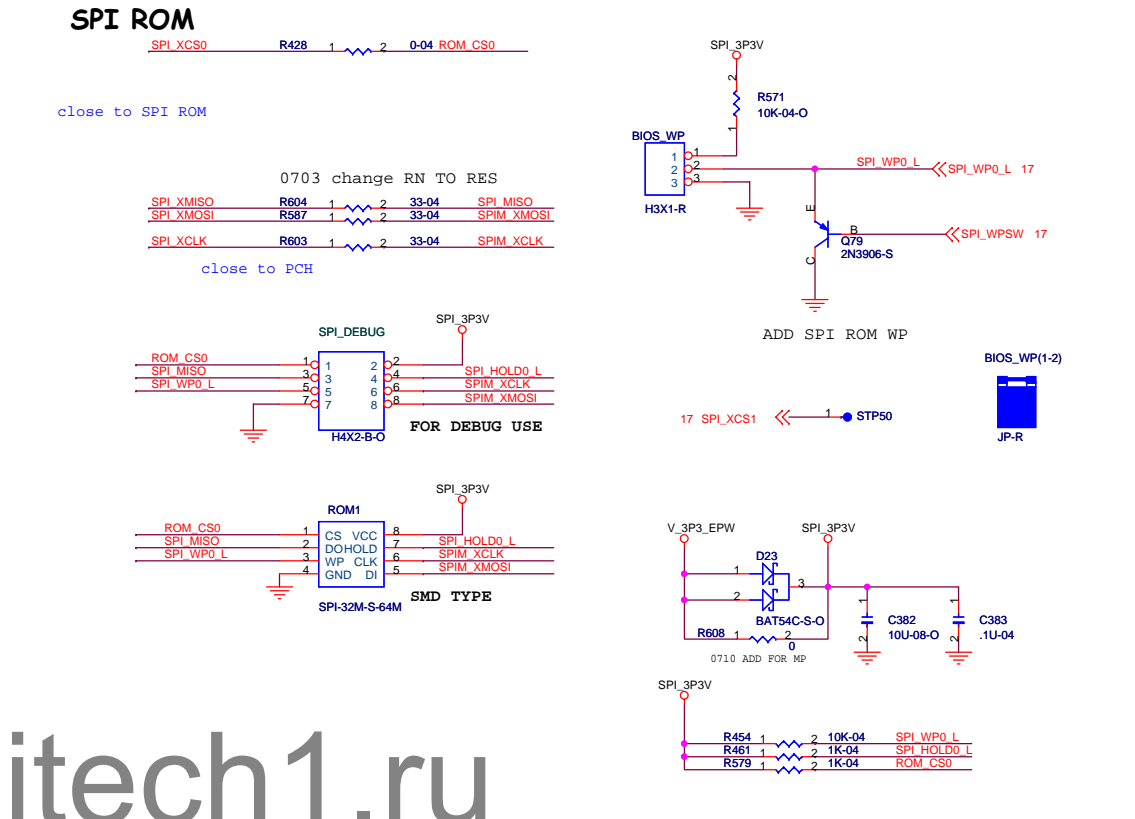
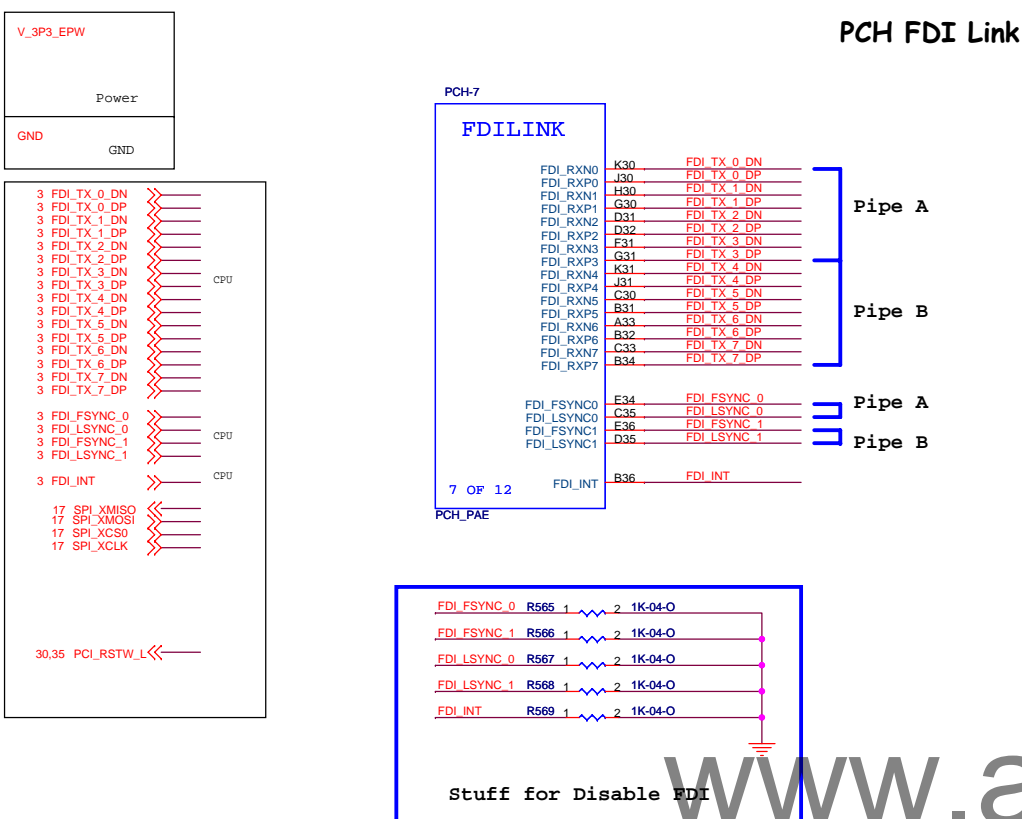
PULL UP

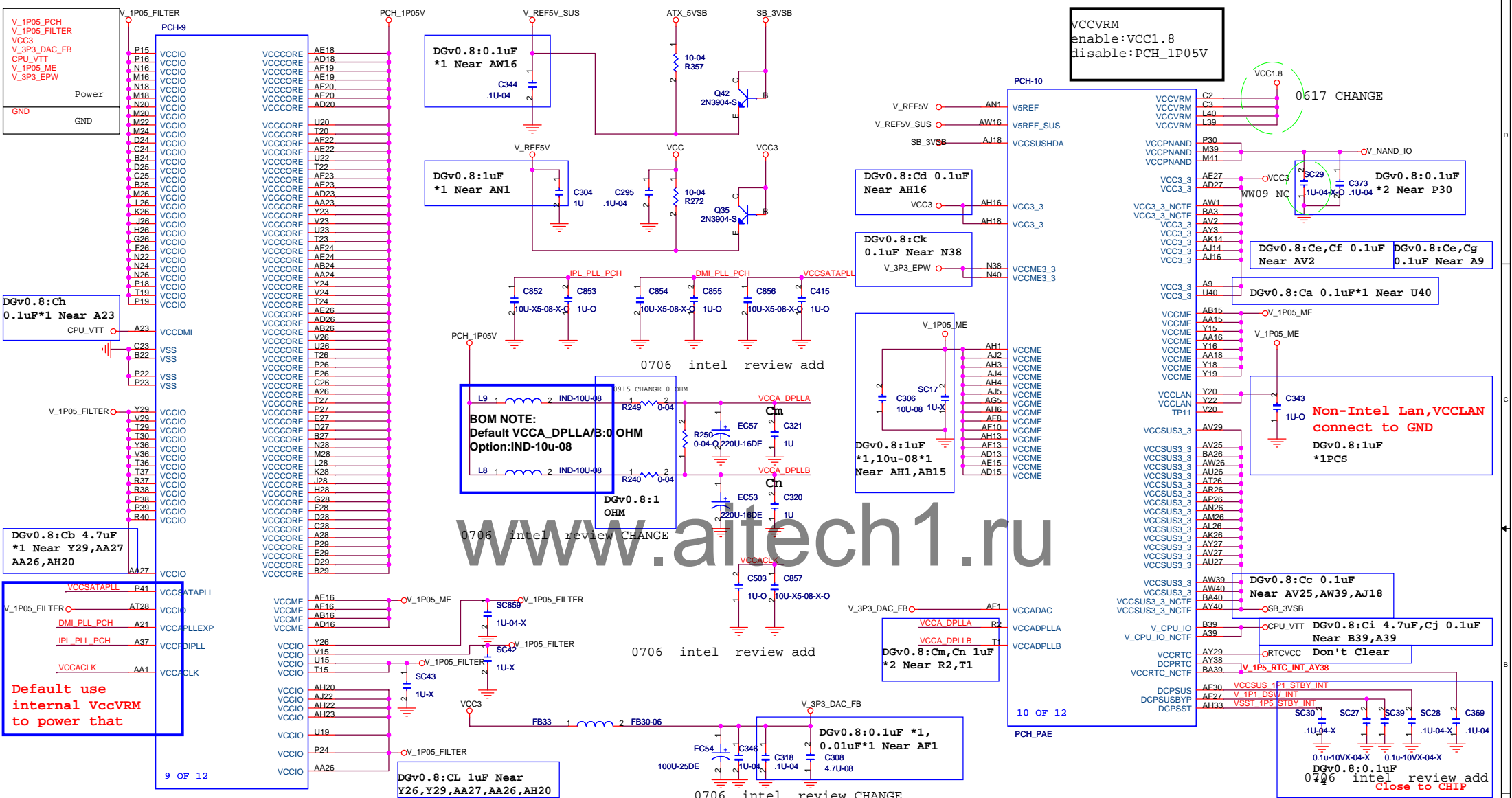
PULL UP



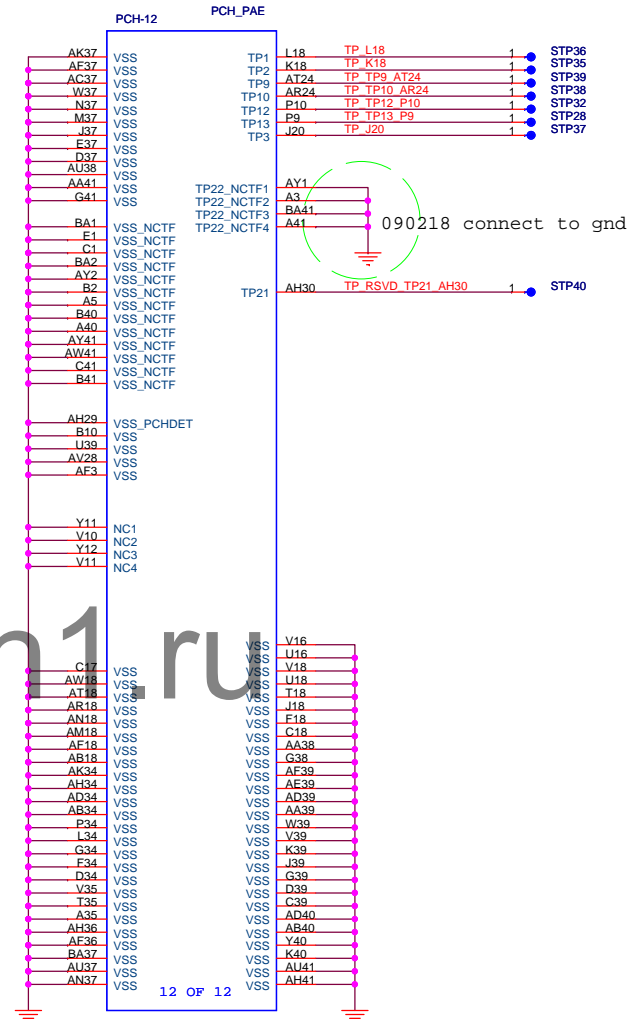
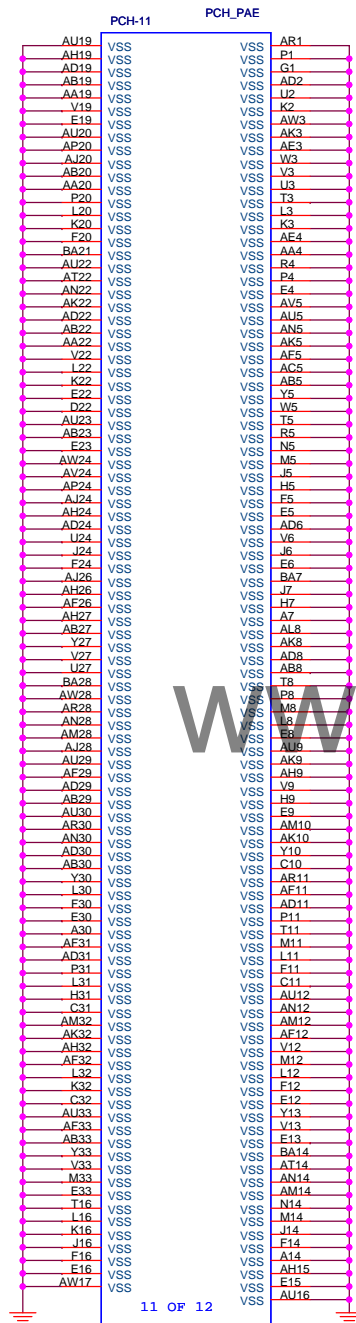


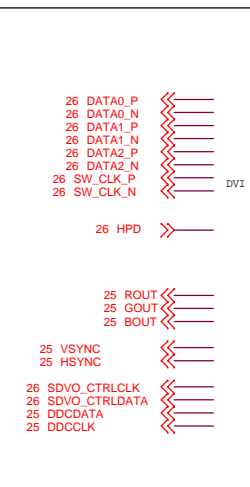
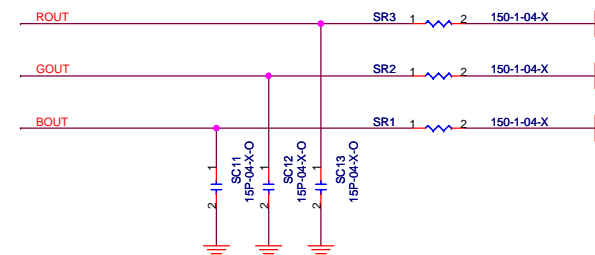




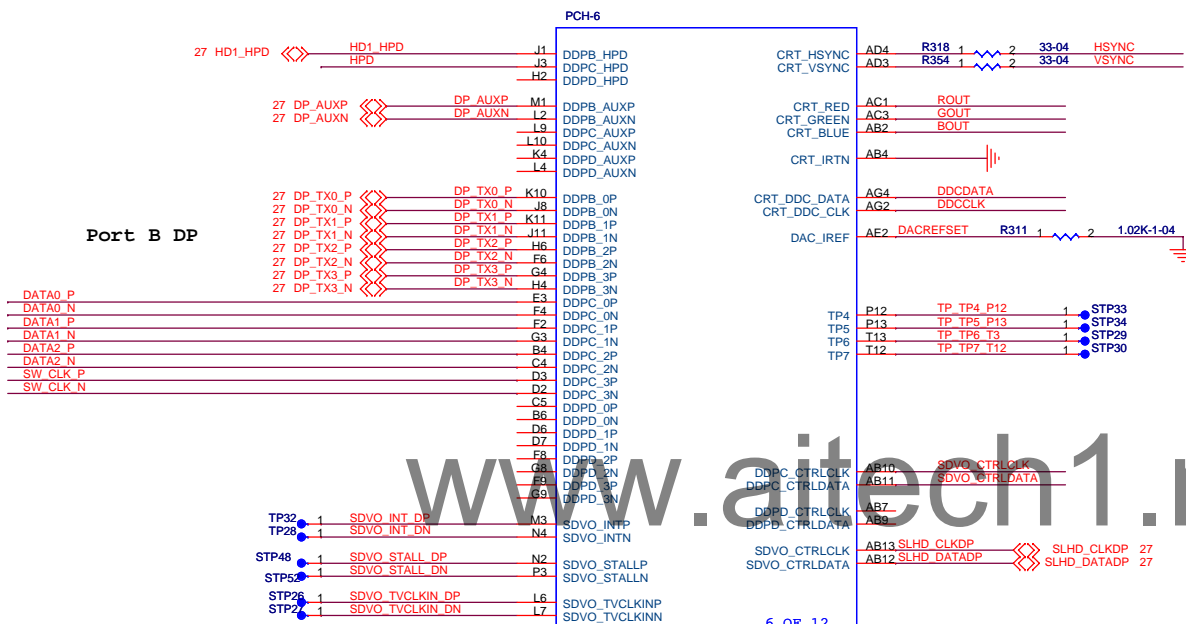


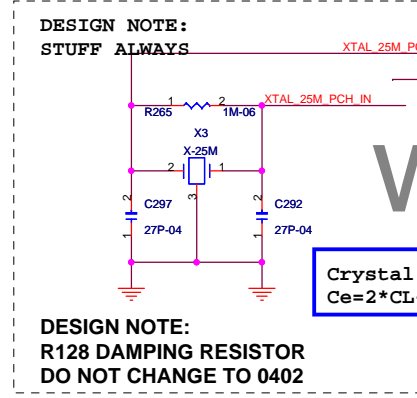
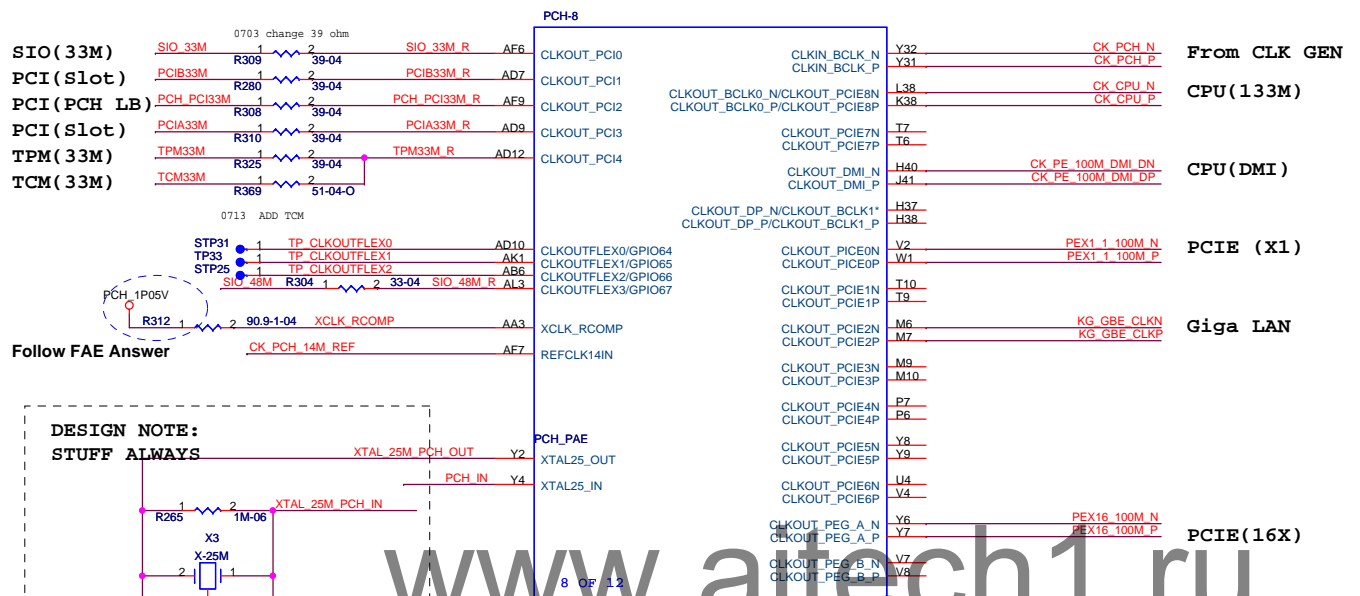
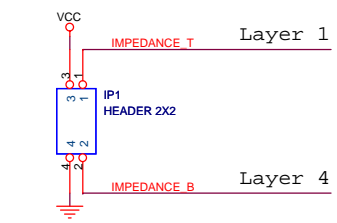
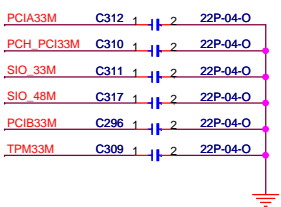
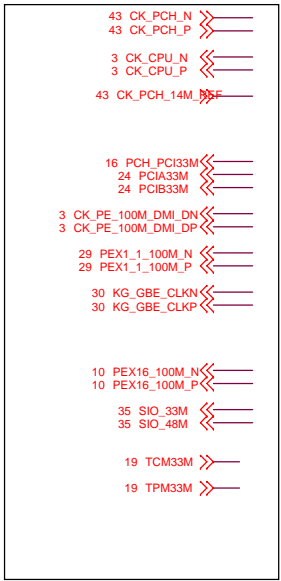
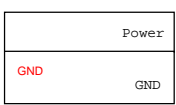
www.aitech1.ru



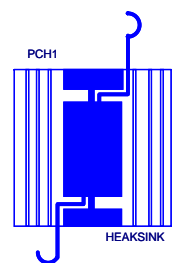


Port C DVI



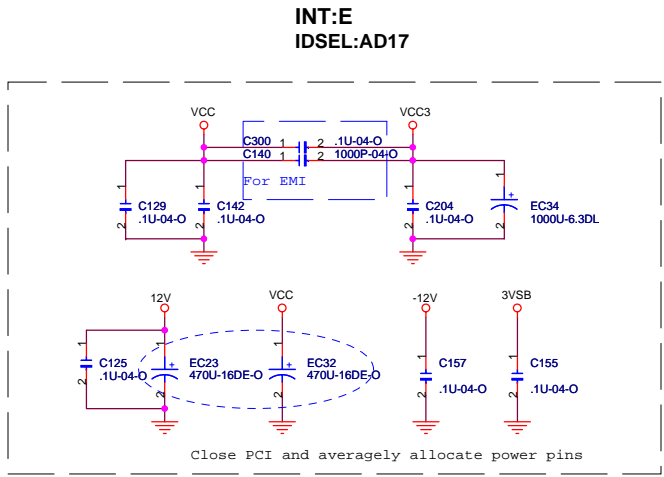
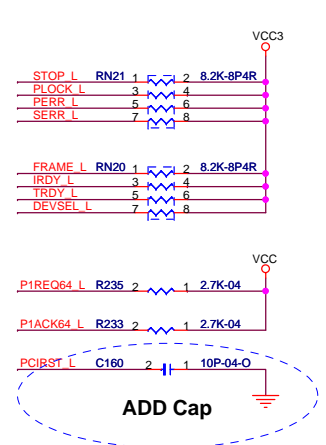
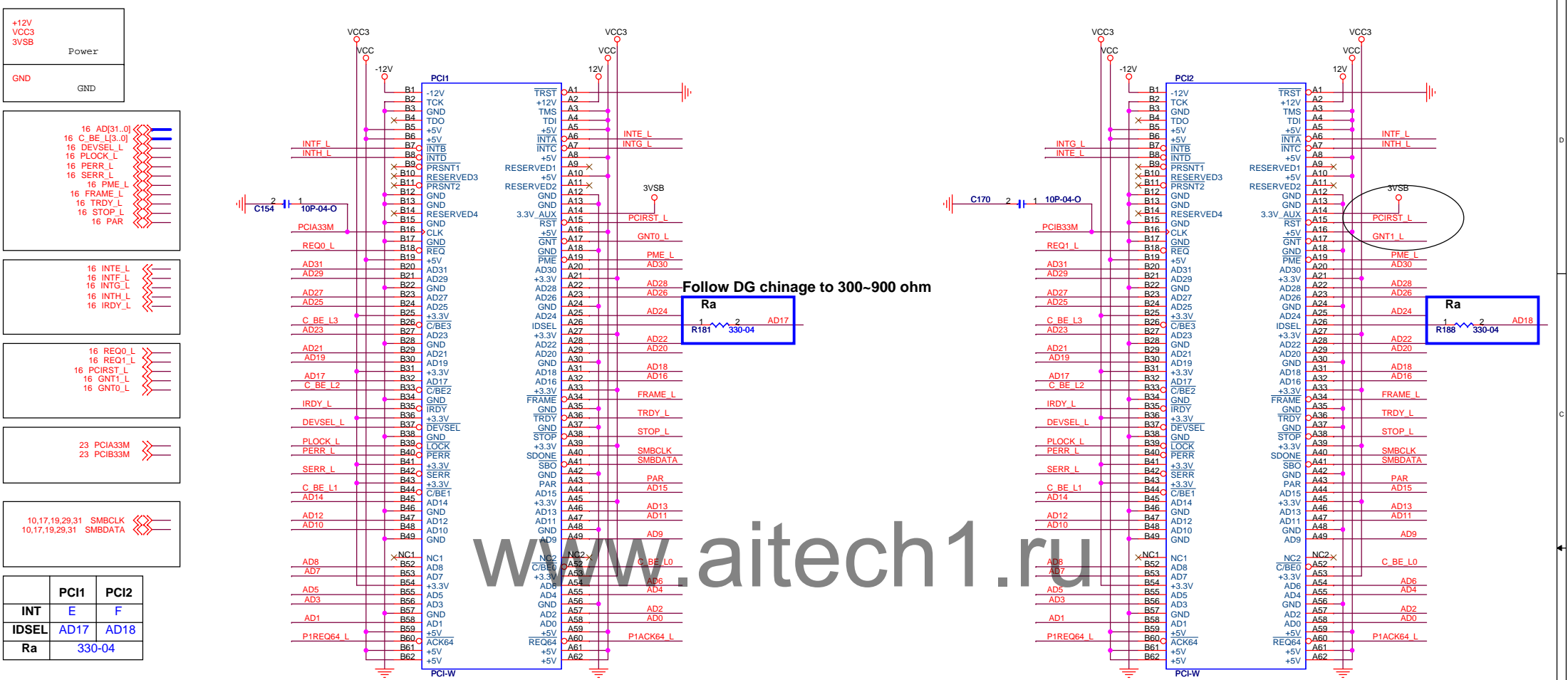


Crystal Spec: +/- 30ppm, CL=20pF
Ce=2*CL (Cs+Ci)

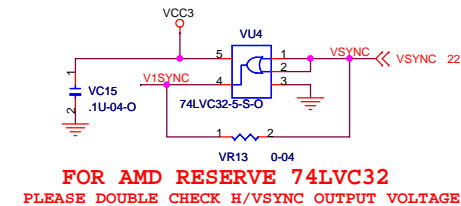
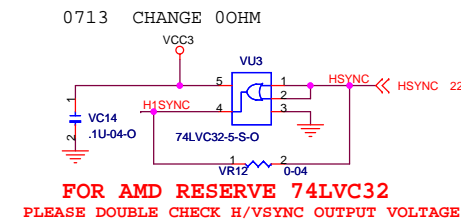
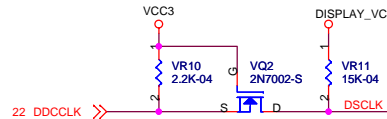
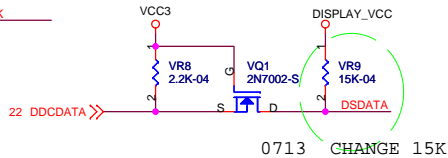
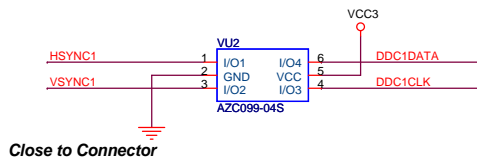
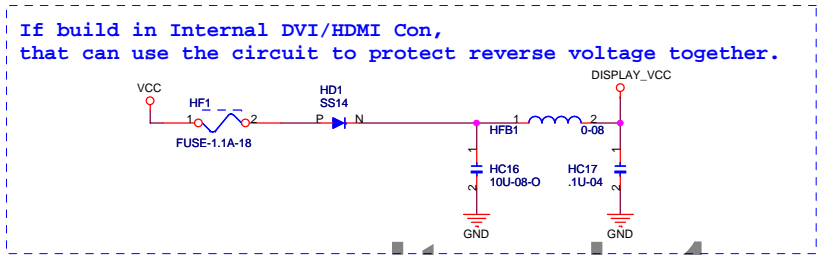
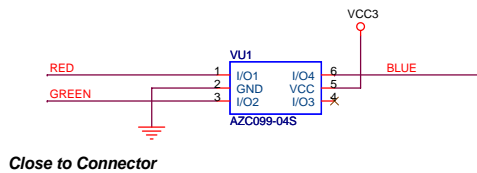
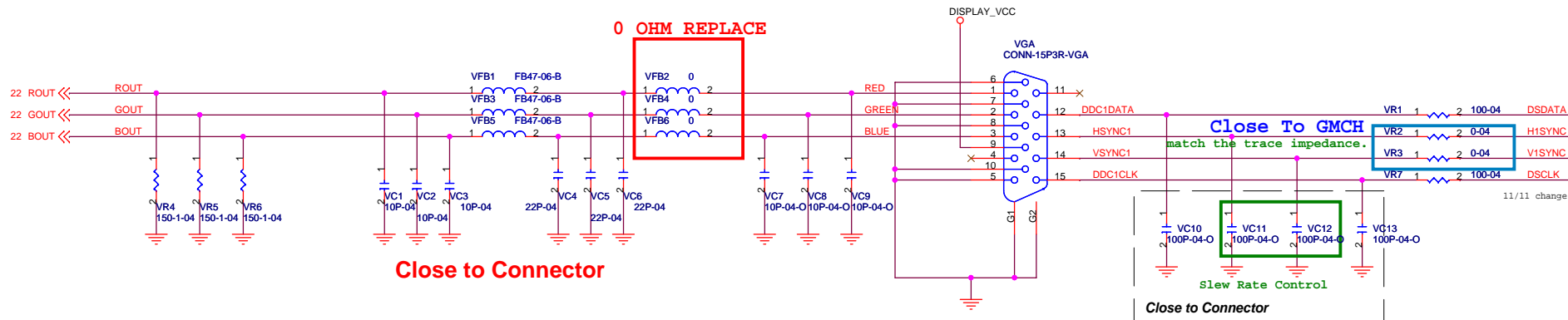


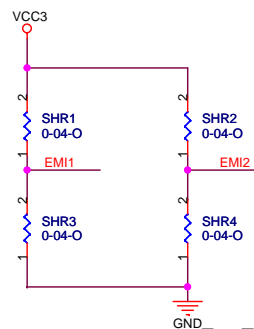
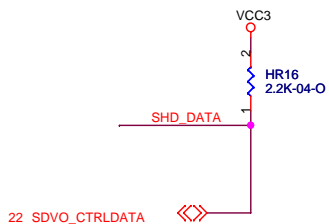
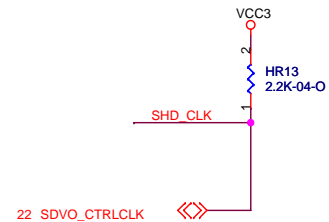
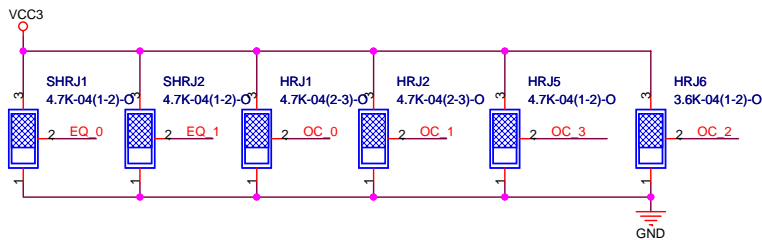
Main Part:20-120-010772

1080 : trace width 4 mil 50 ohm
Trace Length 3150 mils
Spacing: 1.clearance to itself 50/4/50(S:W:S)
2.clearance to other signal 3W



VGA Connector

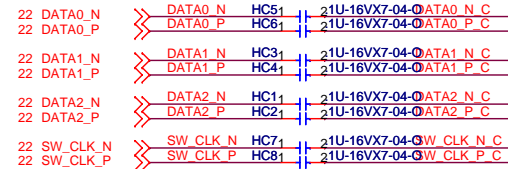




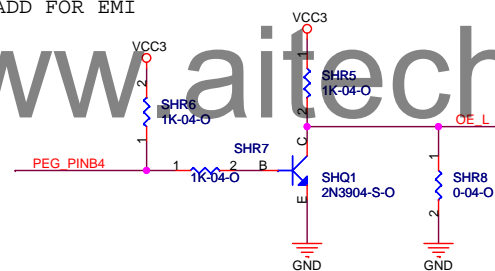
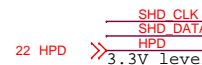
0918 ADD FOR EMI

	PS8101	PI3VDP411LSTZDES
EQ_0	RESERVE 4.7K PULL UP	RESERVE 4.7K PULL DOWN
EQ_1	RESERVE 4.7K PULL UP	RESERVE 4.7K PULL DOWN
OC_0	4.7K PULL UP	RESERVE 4.7K PULL DOWN
OC_1	RESERVE 4.7K PULL UP	RESERVE 4.7K PULL DOWN
OC_2	499 1% OHM PULL DOWN	
OC_3	NC	

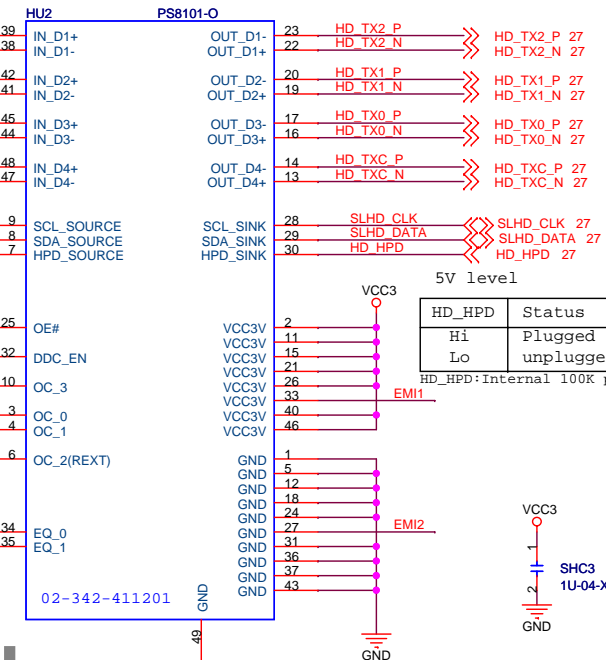
Level shifter noise issue



DDC_EN	Passgate
3.3V	Enable
0	Disable



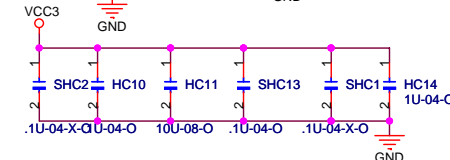
Level Shifter



5V level

HD_HPDP	Status
Hi	Plugged
Lo	unplugged

HD_HPDP:Internal 100K pull low



OC_3	OC_2	OC_1	OC_0	Vswing (mV)	Pre/De-emphasis
0	0	0	0	500	0
0	0	0	1	600	0
0	0	1	0	750	0

EQ_0	EQ_1	Equalization (dB)
0	0	3
0	1	7.2
1	0	10
1	1	20

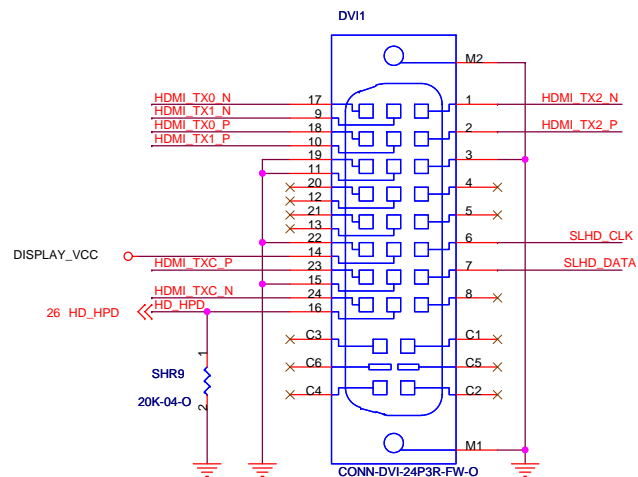


Elitegroup Computer Systems

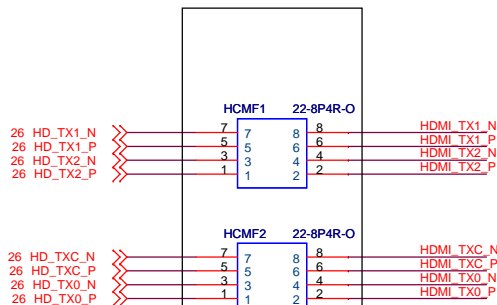
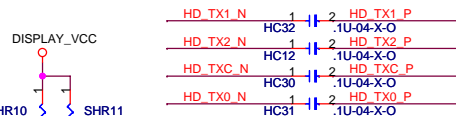
Title **DVI Interface (Switch, Level shifter)**

Size Custom Document Number **Q57H-AM** Rev 1.0

Date: Monday, October 18, 2010 Sheet 26 of 46

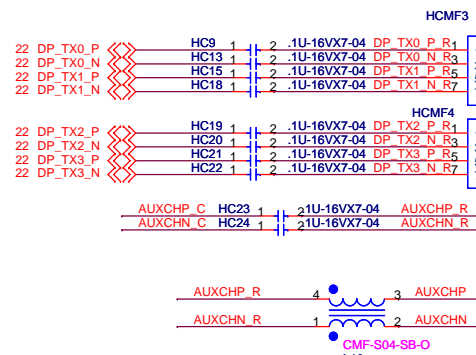


11/09 ADD

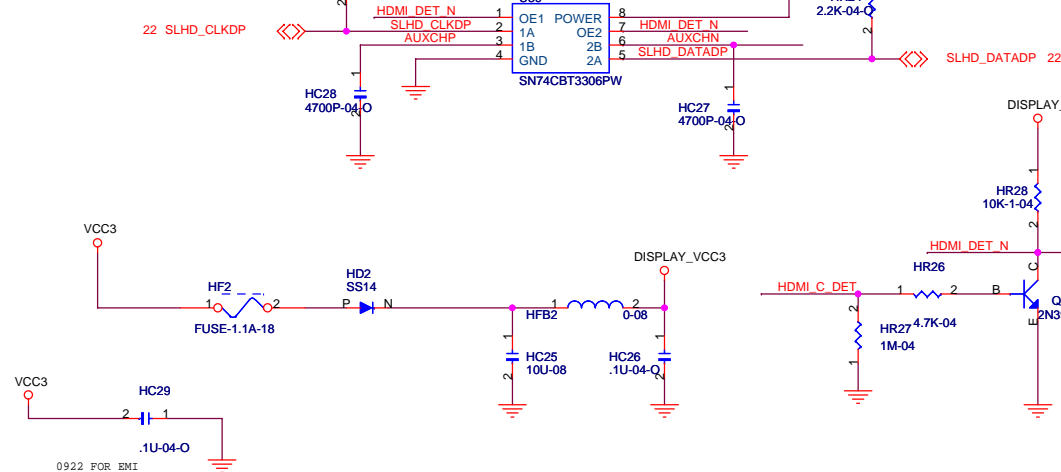
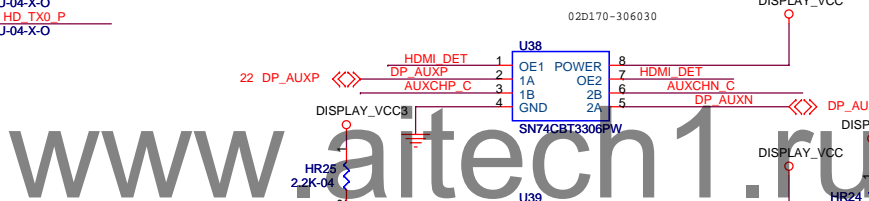


11/13 CHANGE

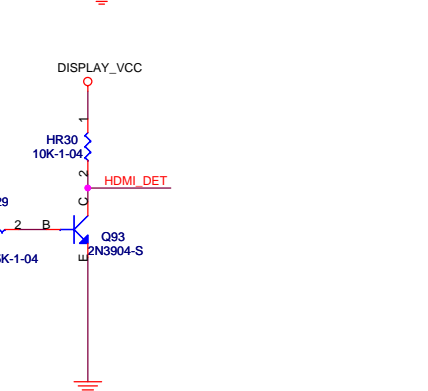
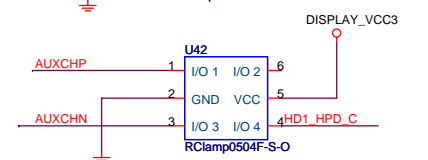
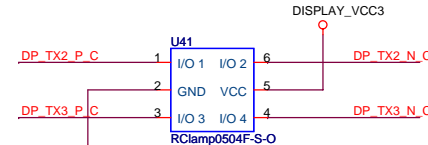
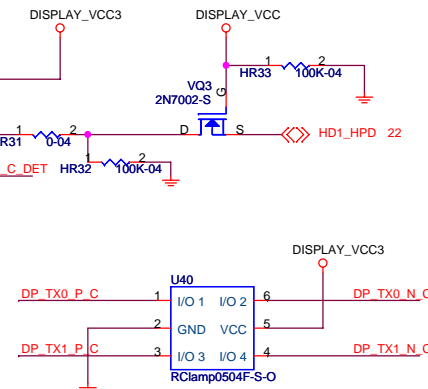
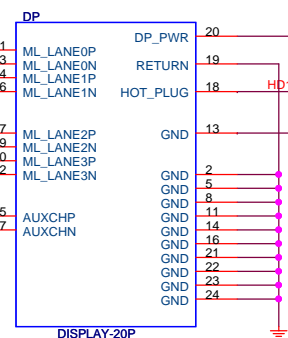
CO-Lay COMMON CHOKE 8P4R

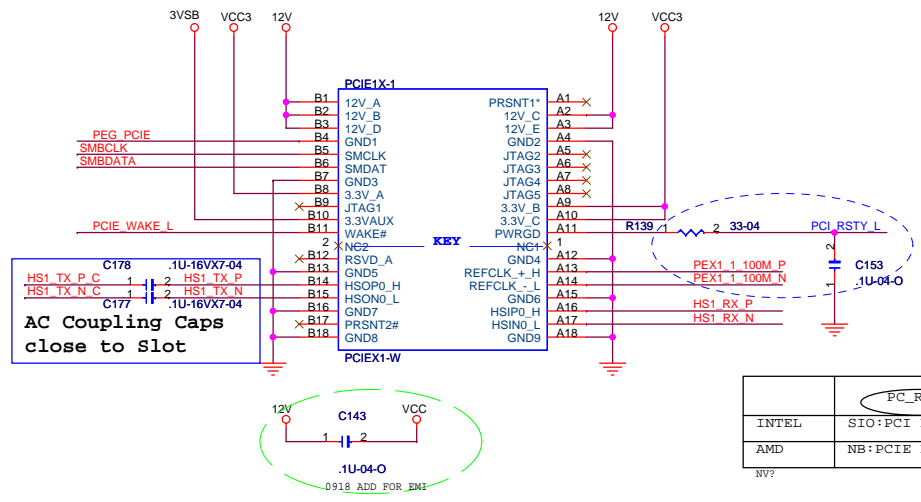
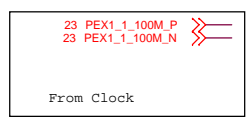
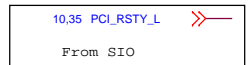
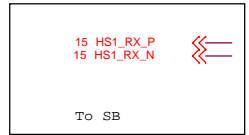
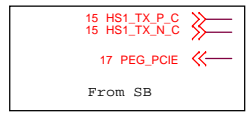
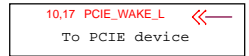
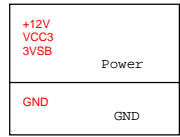
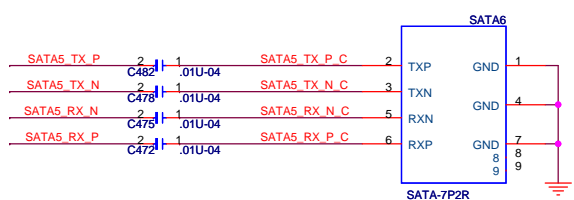
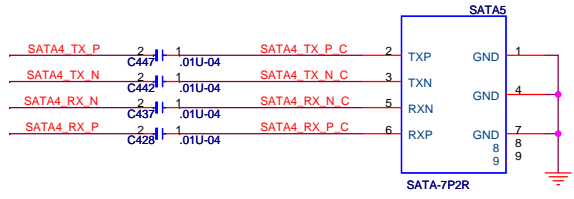
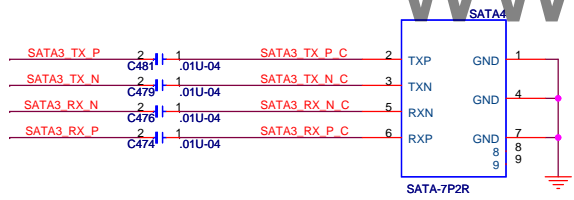
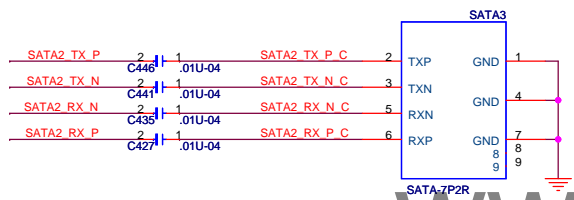
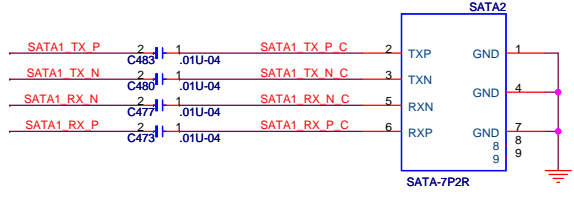
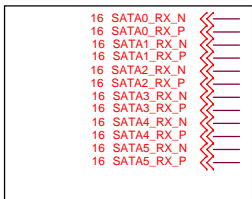
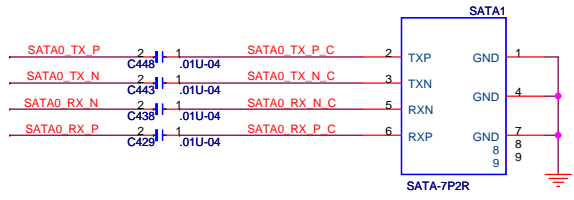
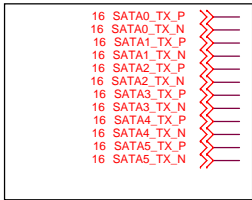


0706 intel review change



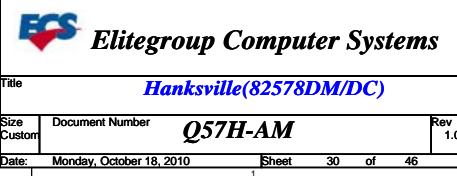
0922 FOR EMI



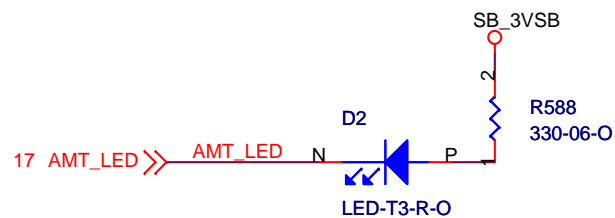


	PC_RST
INTEL	SIO:PCI REST
AMD	NB:PCIE REST
NV?	

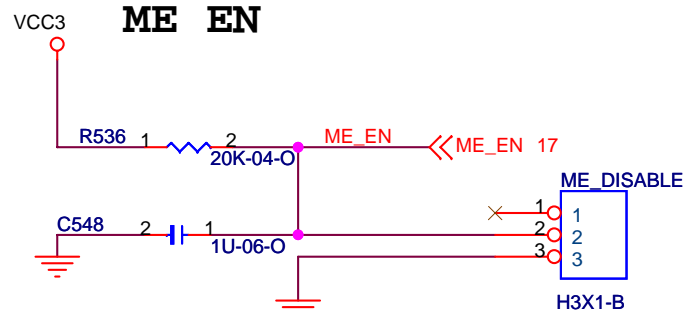
www.aitech1.ru



AMT_LED



ME EN



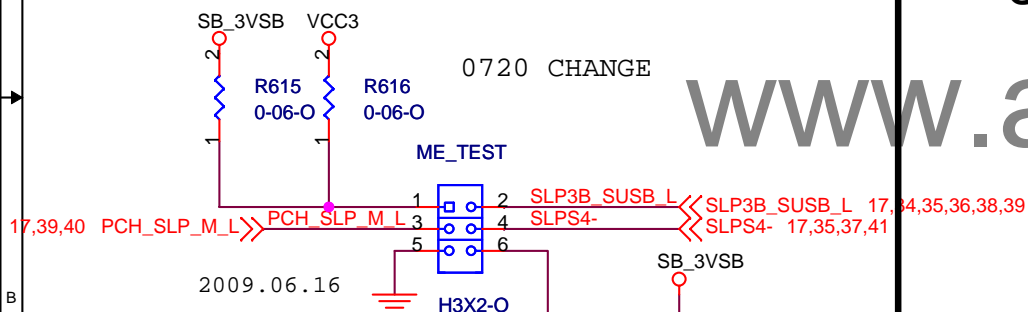
ME_DISABLE(1-2)



ME EN Clear Header

	ME EN
* 1-2	NORMAL
2-3	ME_DI

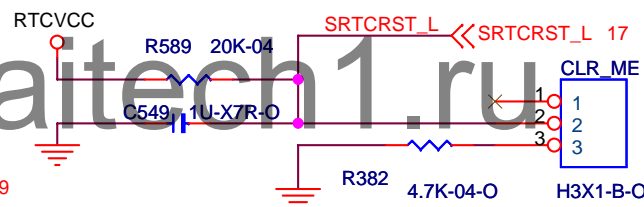
ME_TEST



0701 ME TEST

- 16,17,28,34,35 PWROK >> 1 STP24
- 17 RSMRST >> 1 STP74
- 17,39 SLP_LAN_L >> 1 TP8
- 16 PCH_MEPWROK_R >> 1 STP46
- 17,34 SLP5_L >> 1 STP44
- 17,39,40 PCH_SLP_M_L >> 1 TP4
- 17,34,35,36,38,39 SLP3B_SUSB_L >> 1 TP5
- 17,35,37,41 SLPS4- >> 1 STP41

Clear ME

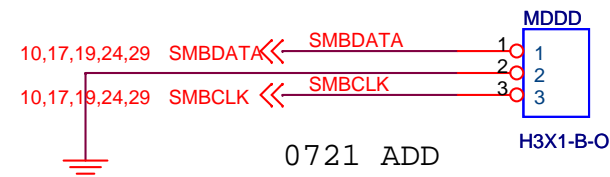


CLR_ME(1-2)



ME Clear Header

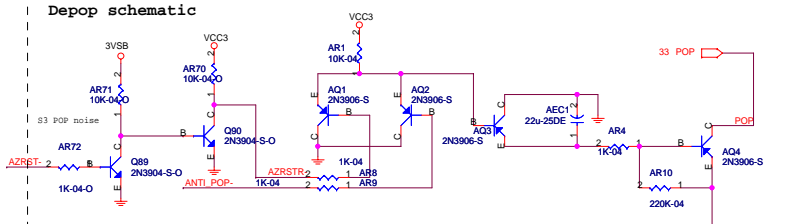
	CLR_ME
* 1-2	NORMAL
2-3	CLEAR ME



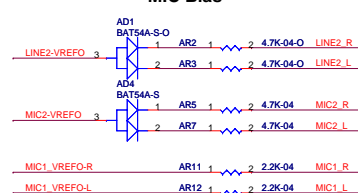
Elitegroup Computer Systems

Title AMT6.0		
Size A	Document Number Q57H-AM	Rev 1.0
Date:	Monday, October 18, 2010	Sheet 31 of 46

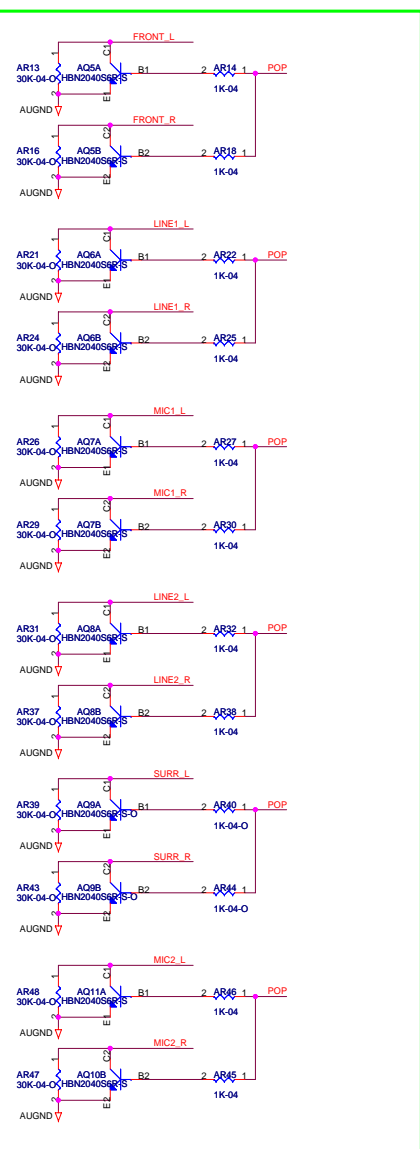
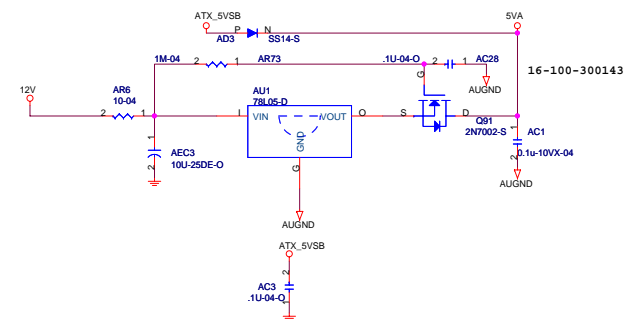
Depop schematic



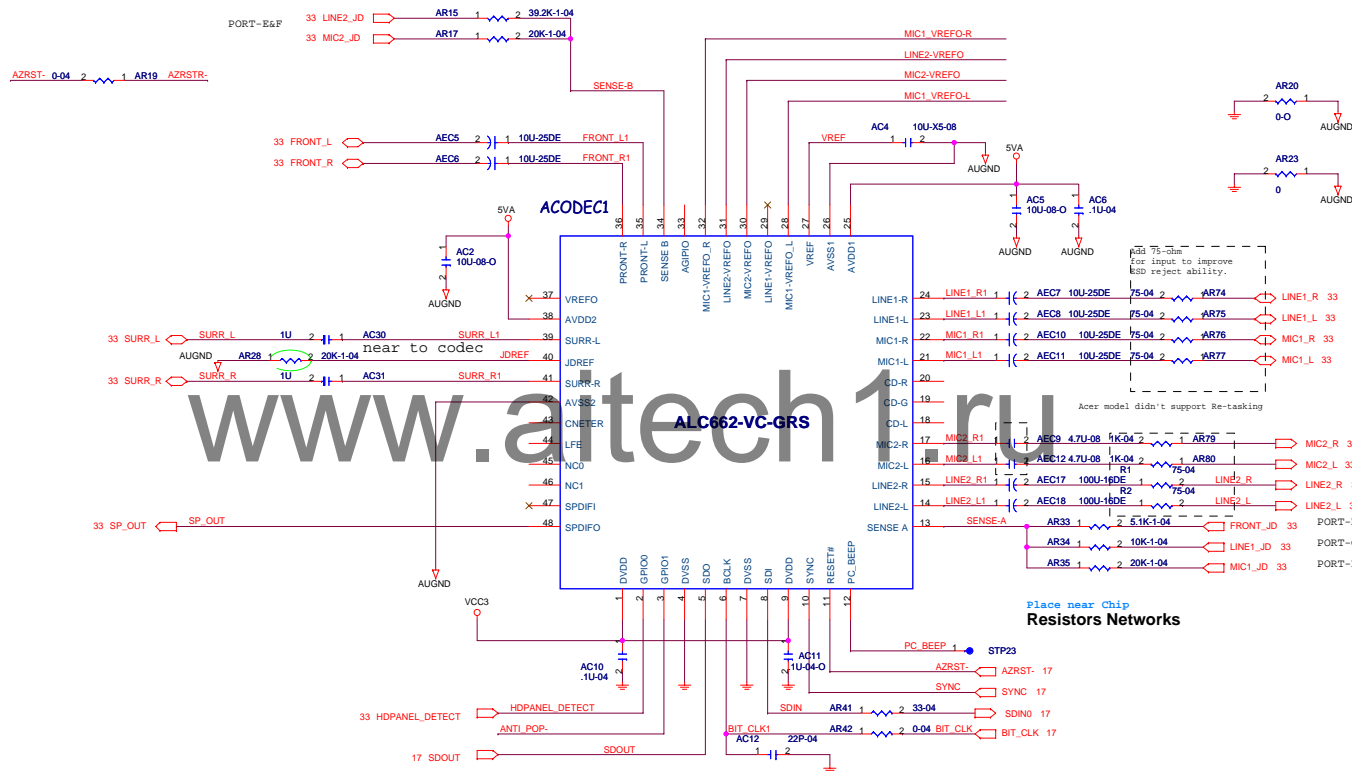
MIC Bias



Improve the background noise of MIC boost



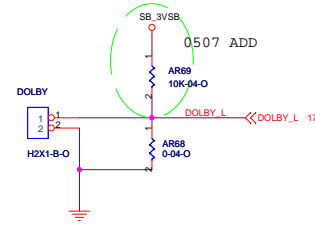
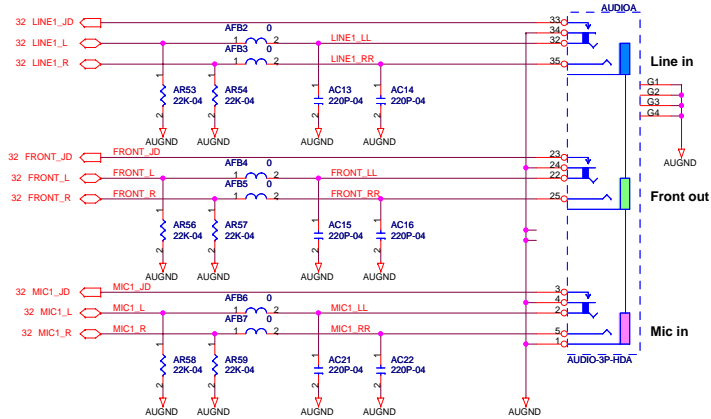
Place near Chip Resistors Networks



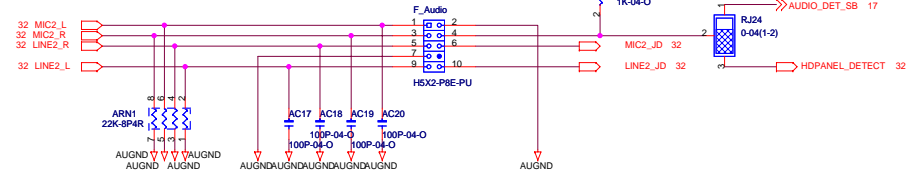
Place near Chip

Resistors Networks

REAR-AUDIO

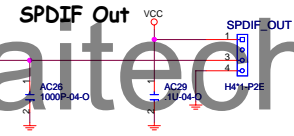


FRONT-AUDIO

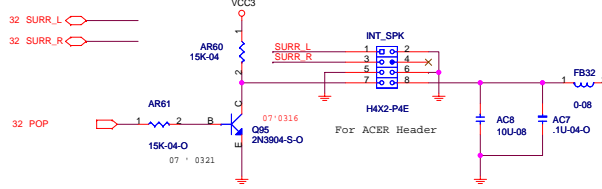


GPI: cable detection	
LOW	Plug cable
HIGH	No plug cable

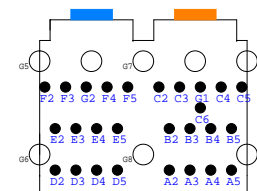
SPDIF IN/OUT



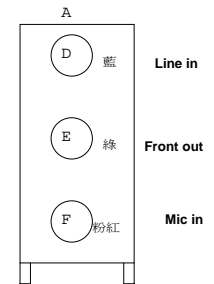
Internal speaker header



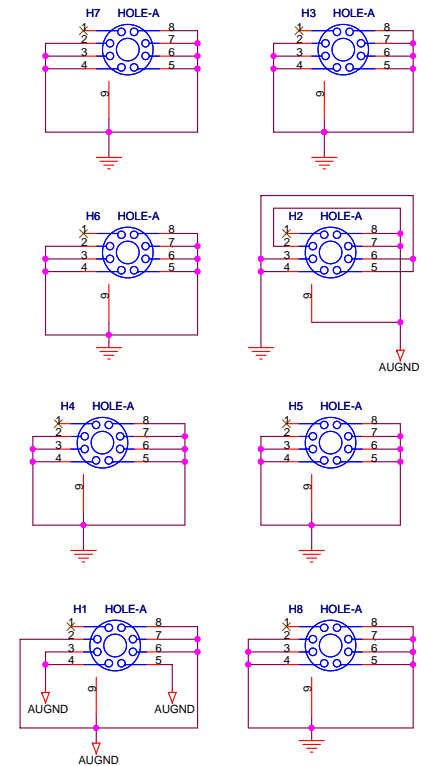
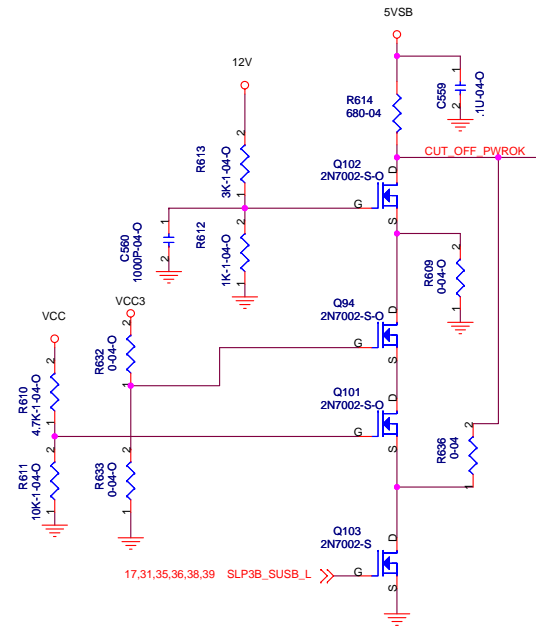
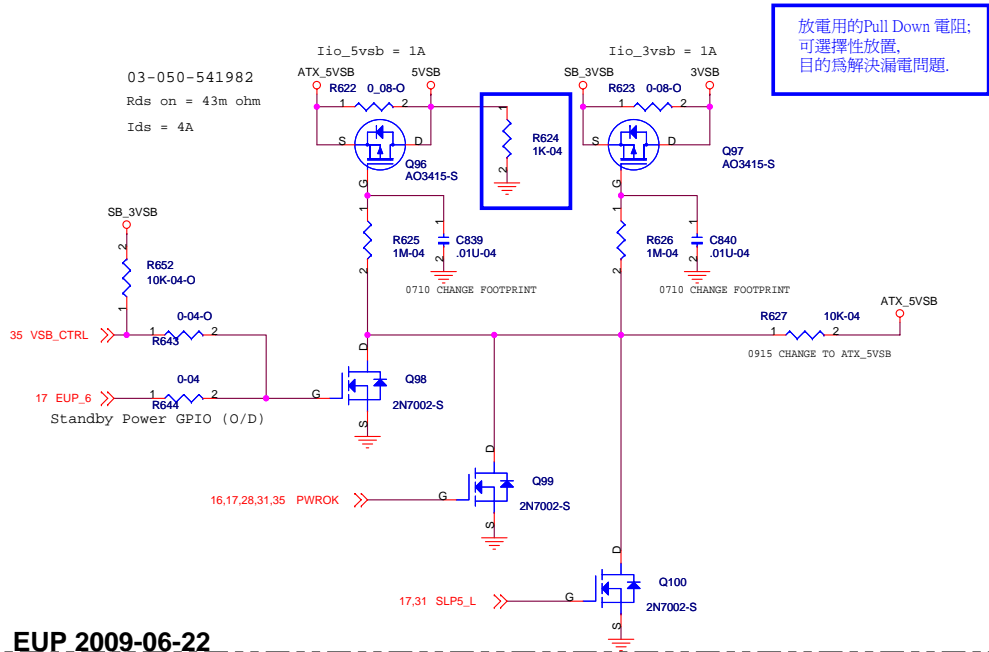
www.aitech1.ru



TOP VIEW



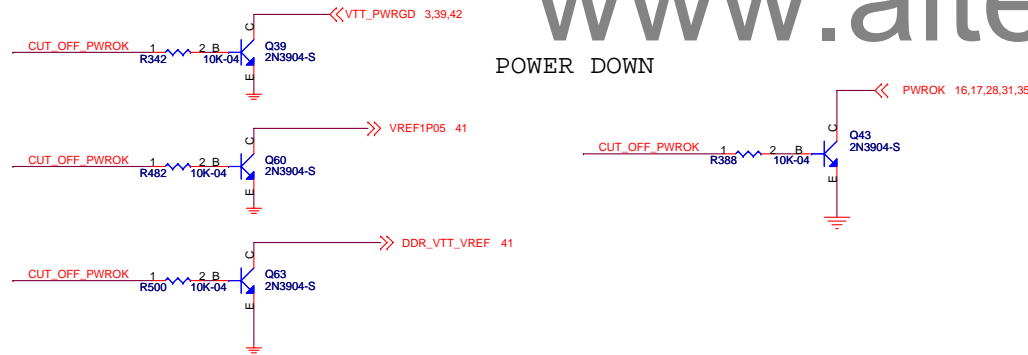
FRONT VIEW

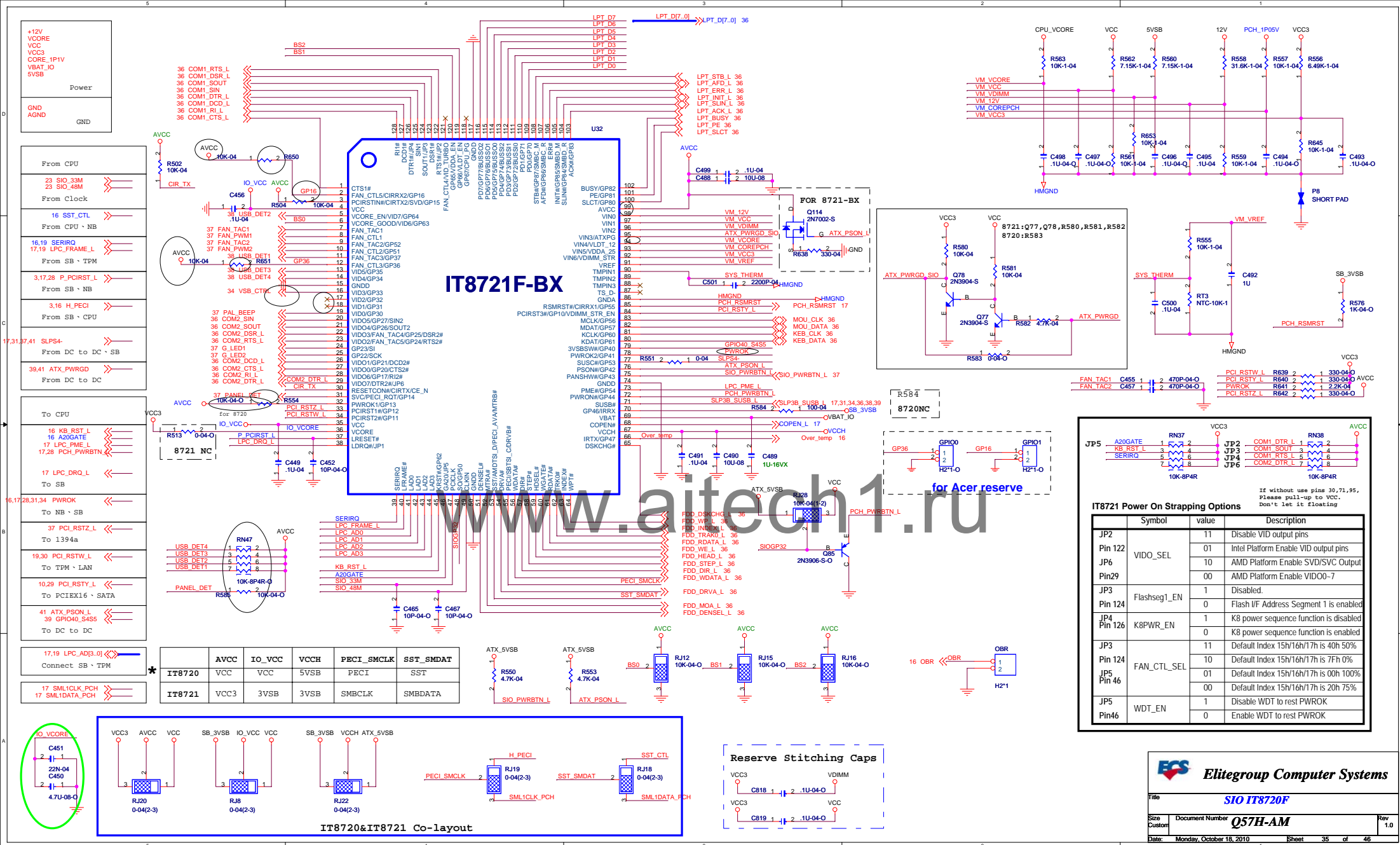


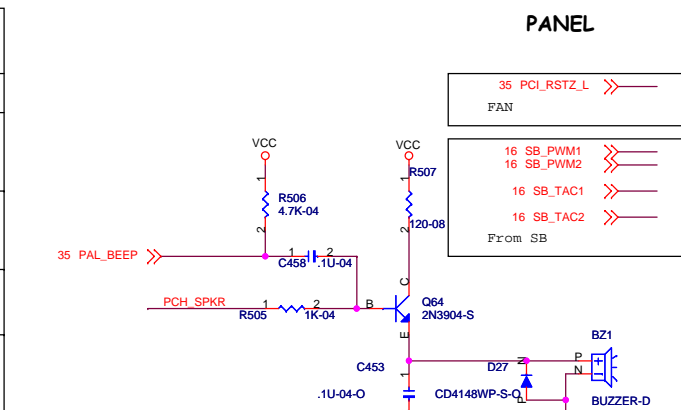
PWROK low to VCC falling
IBEX PEAK 40ns requirement

www.aitech1.ru

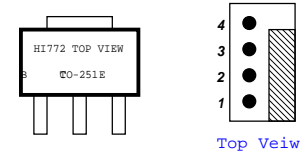
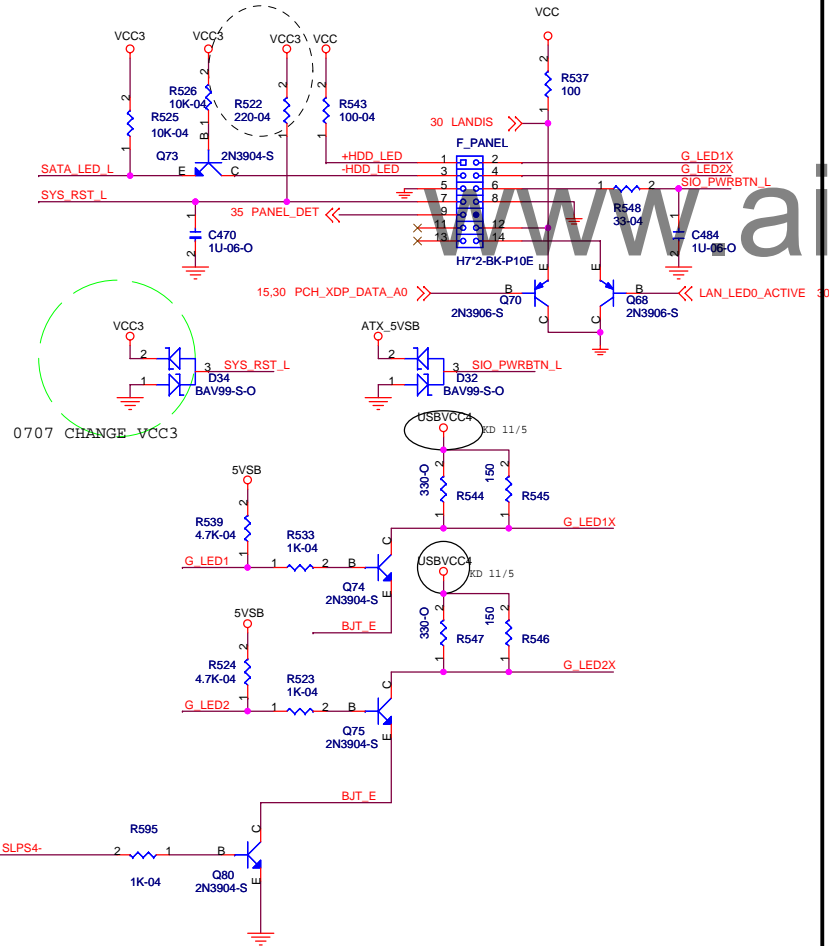
POWER DOWN



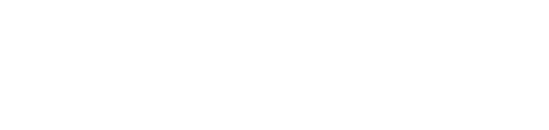
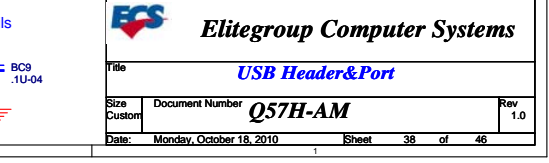
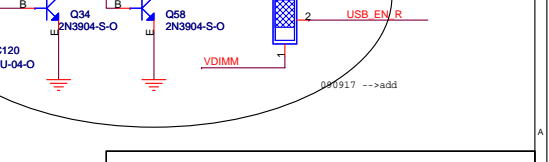
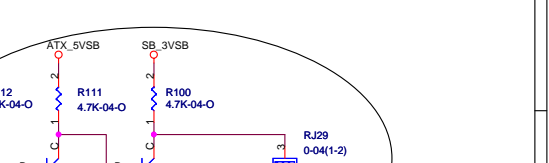
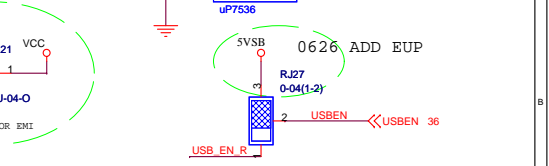
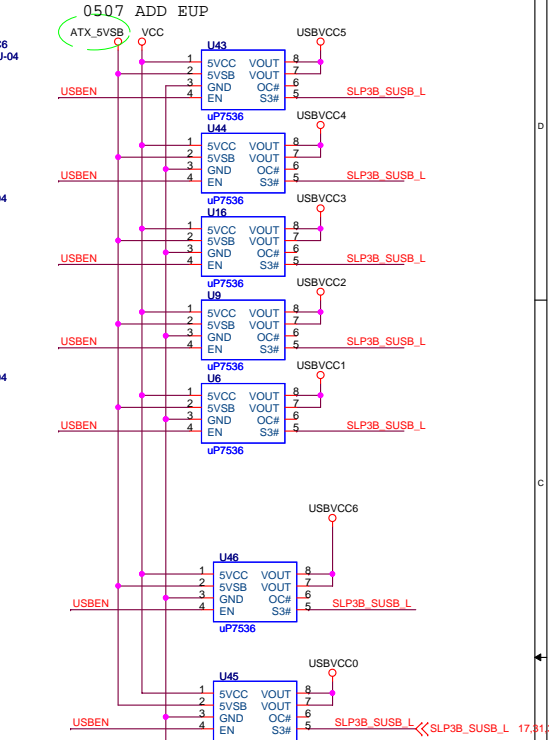
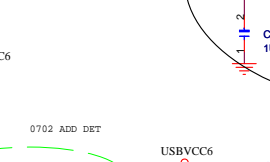
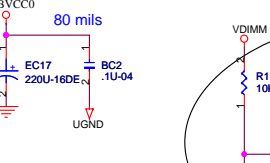
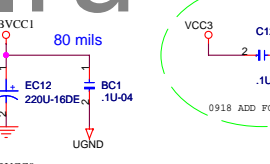
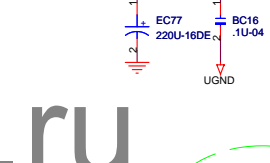
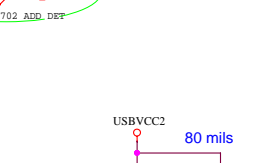
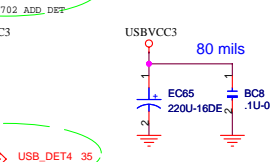
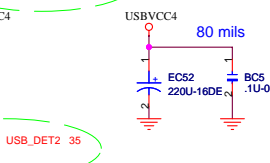
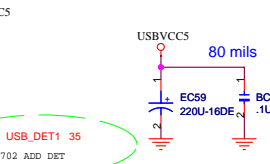
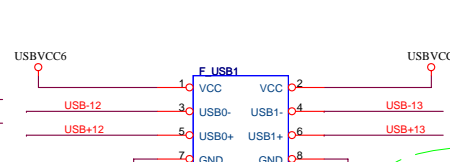
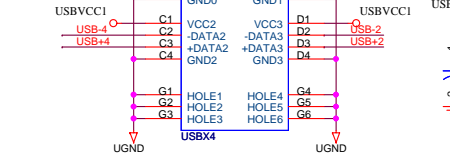
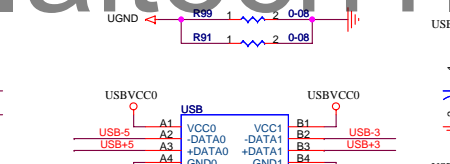
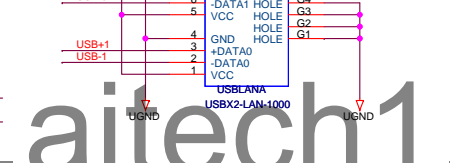
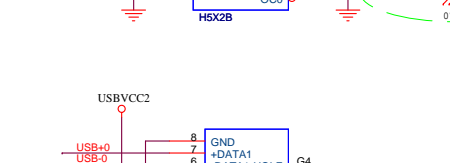
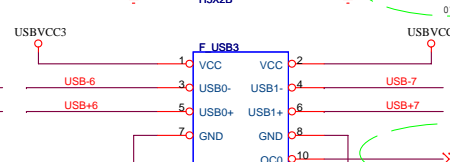
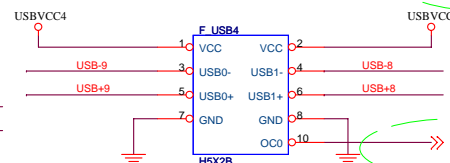
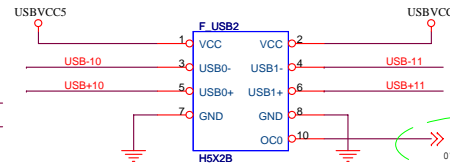
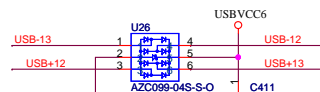
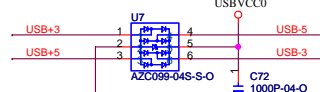
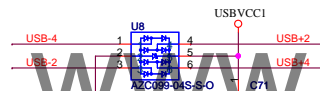
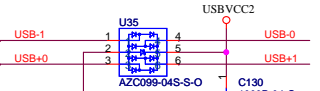
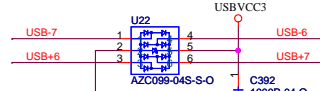
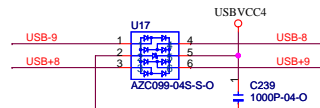
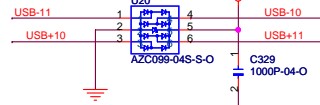
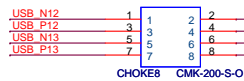
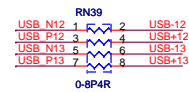
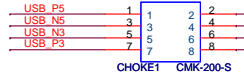
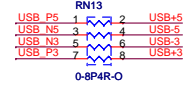
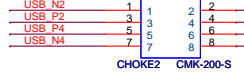
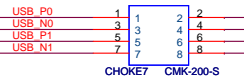
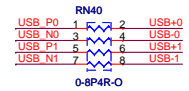
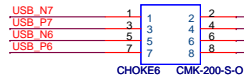
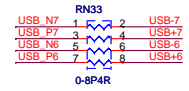
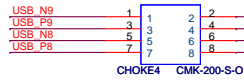
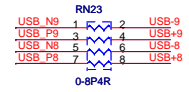
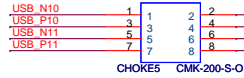
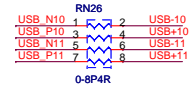




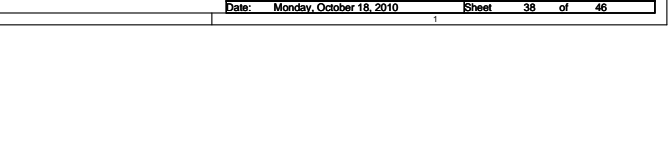
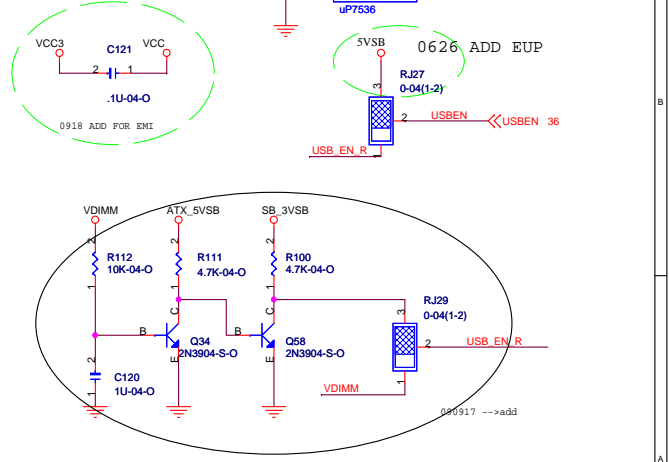
090119
WW51 SYS_RST_L should
pull high to VCC3 not 3VSB and 220 ohm



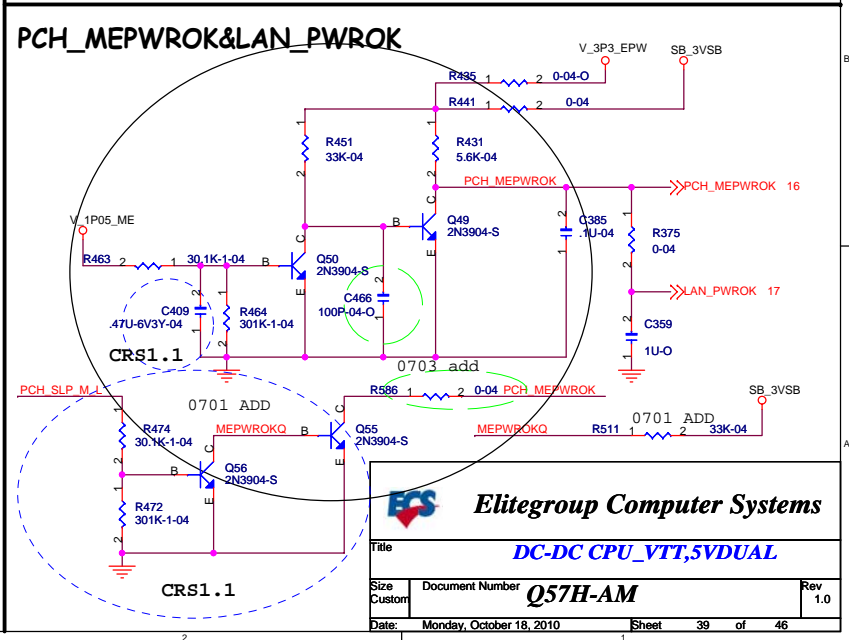
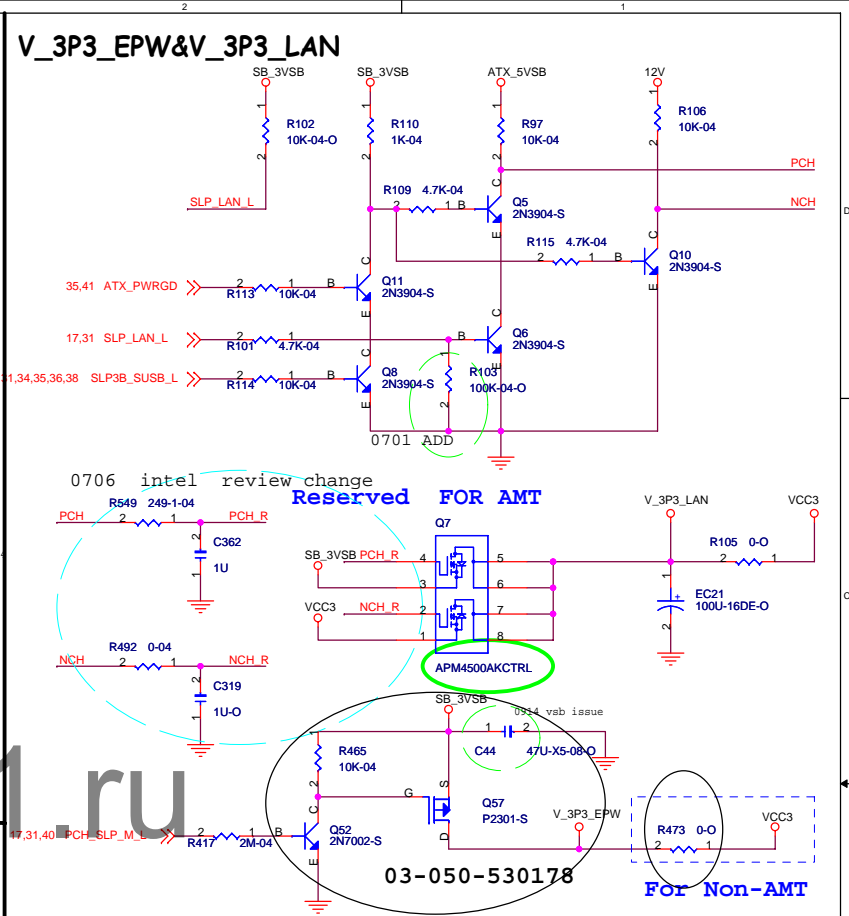
15 USB_P[13..0] >> USB_P[13..0]
15 USB_N[13..0] >> USB_N[13..0]

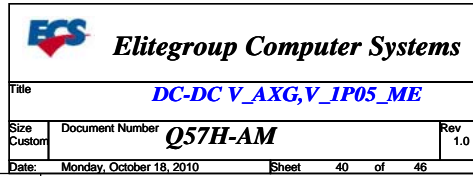


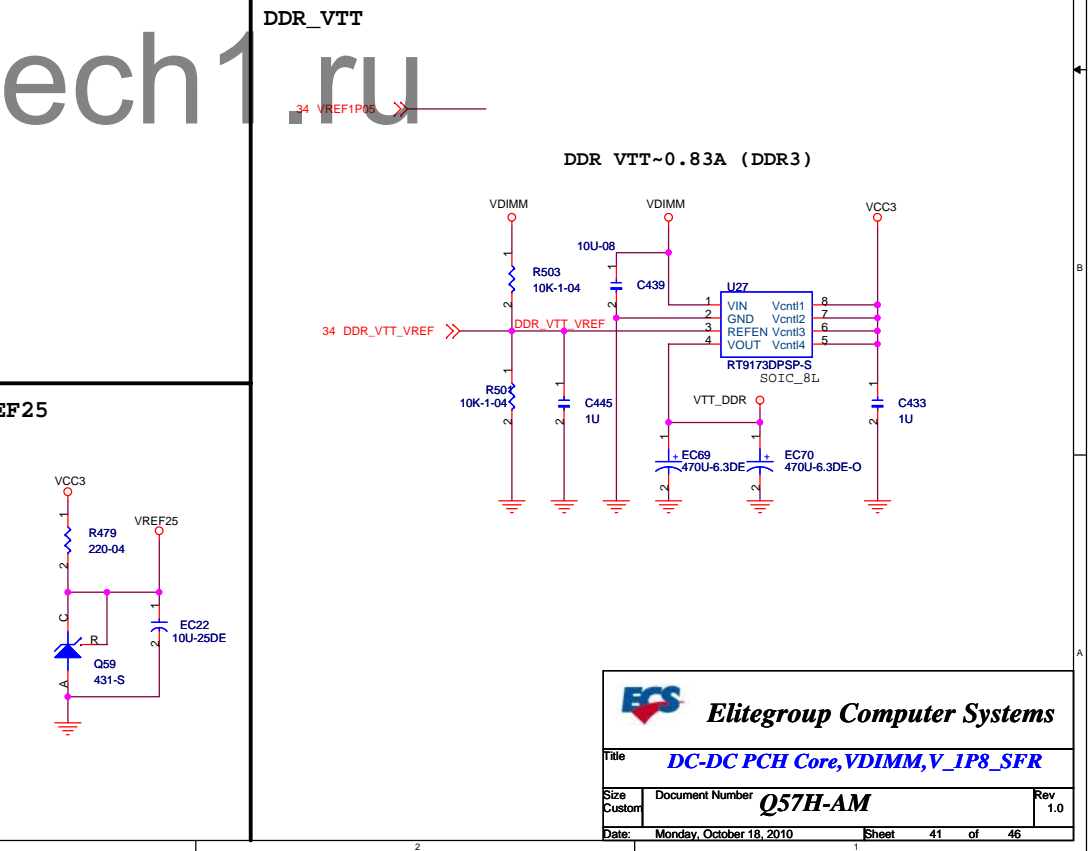
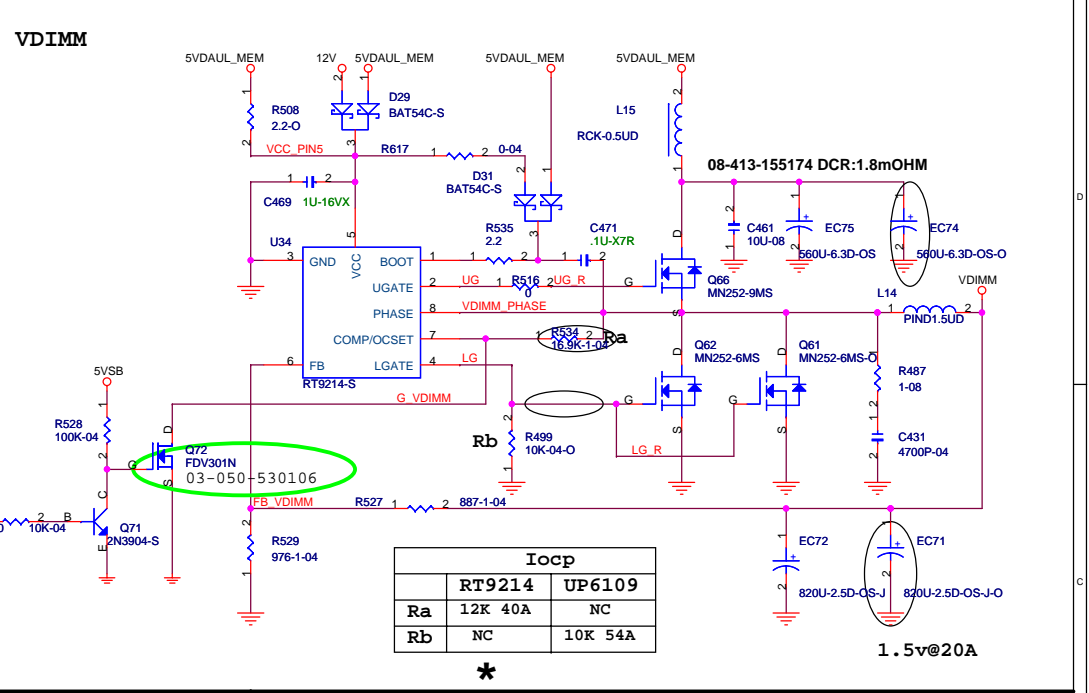
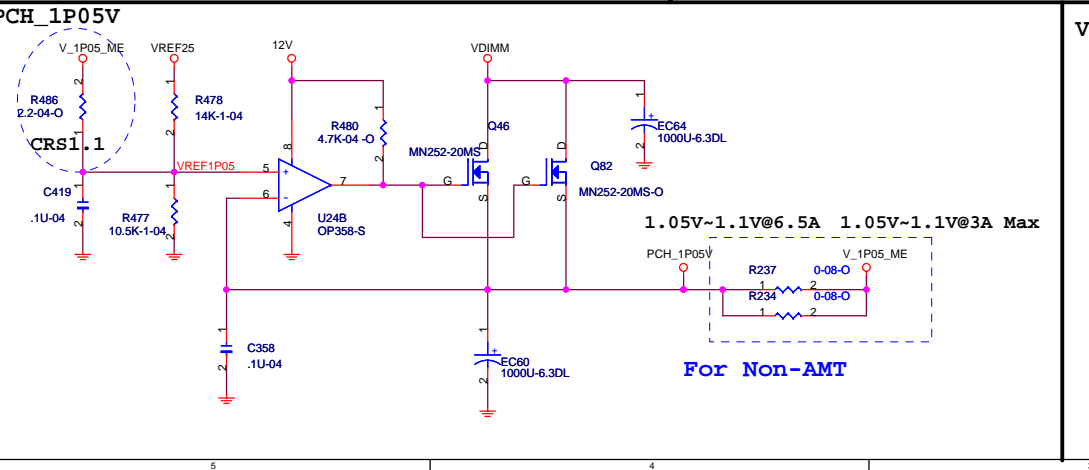
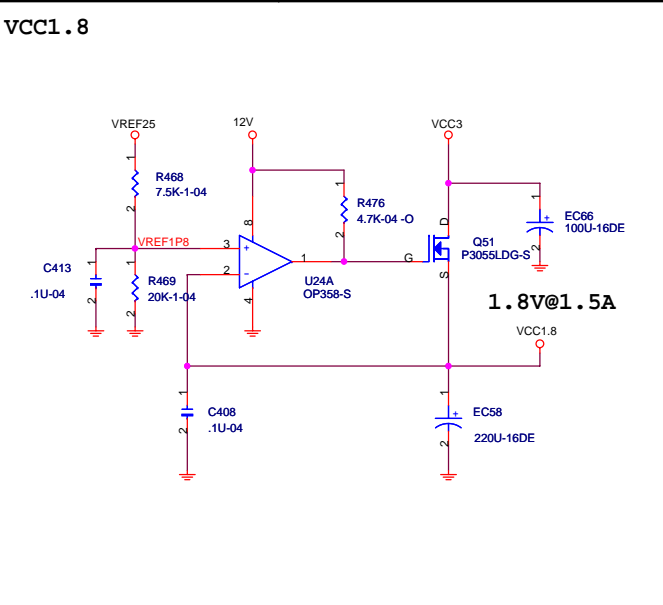
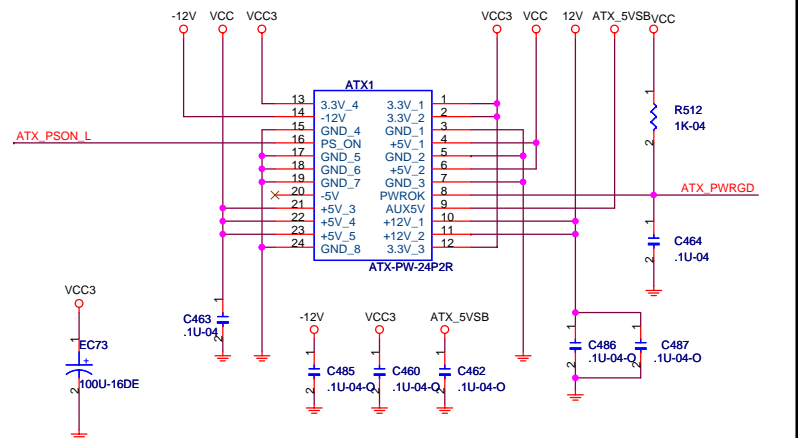
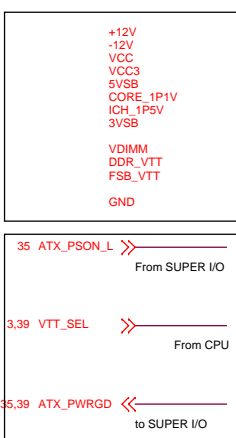
www.aitech1.ru



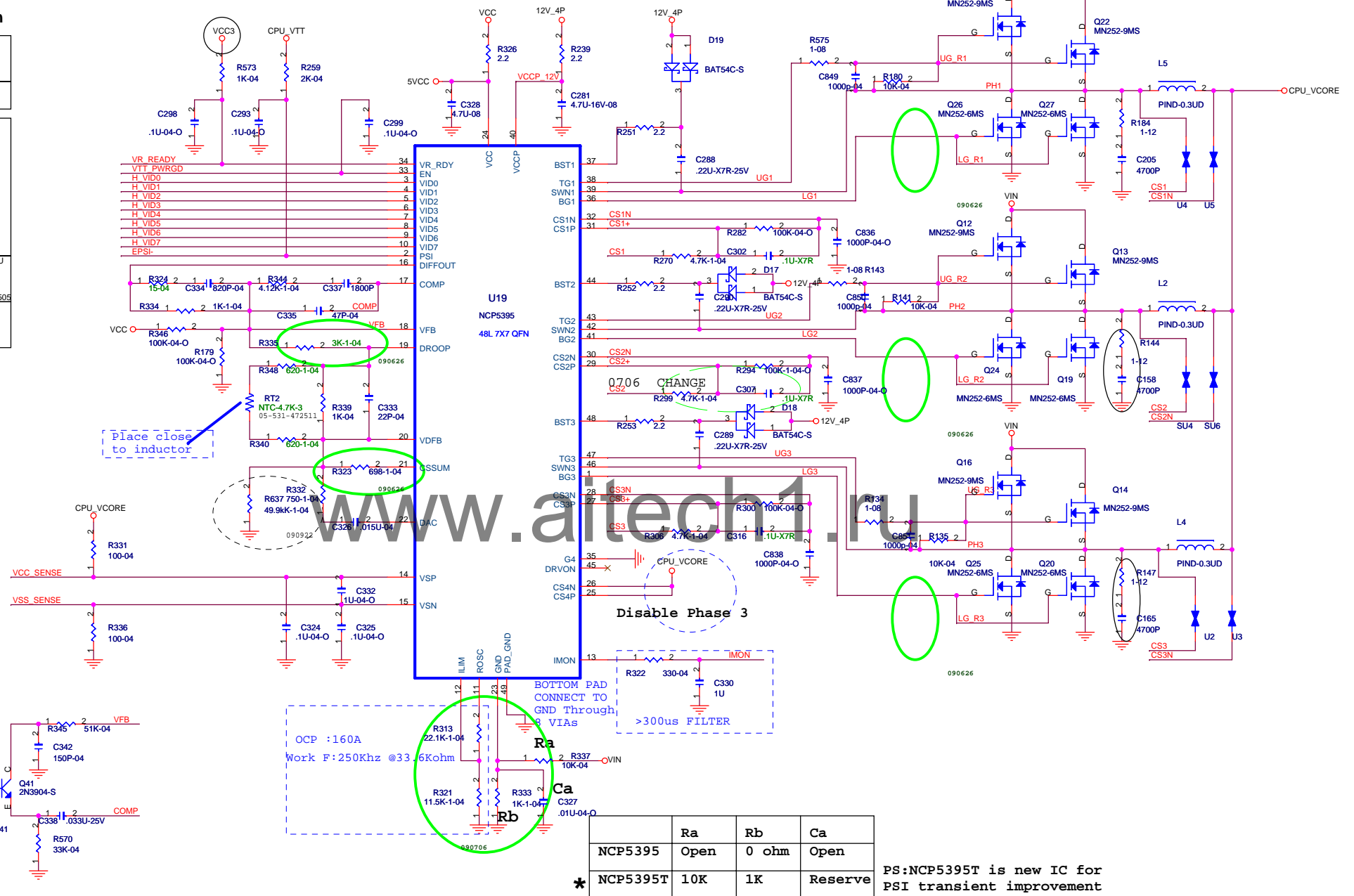
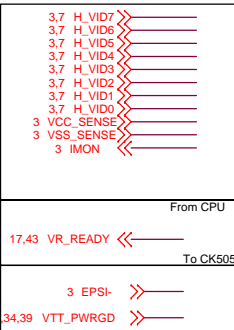
USB Header&Port	
Title	Document Number
Size	Q57H-AM
Date:	Monday, October 18, 2010
Sheet	38 of 46





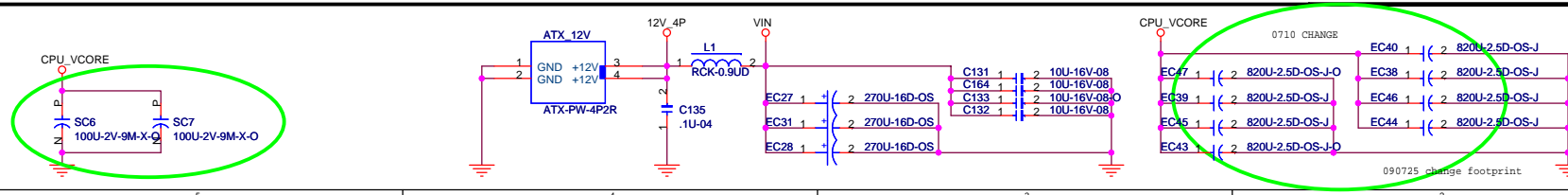


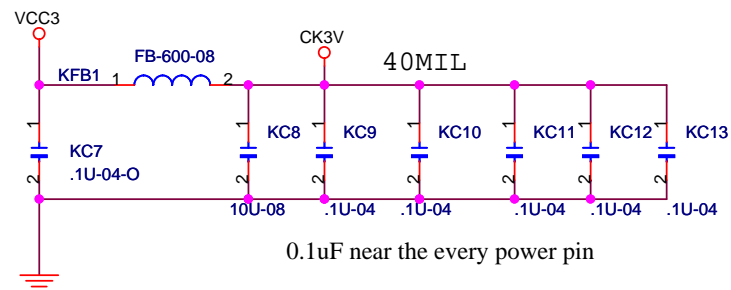
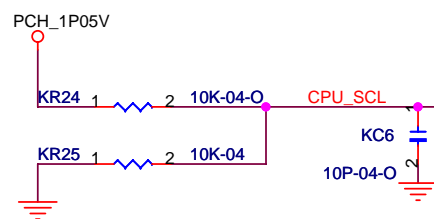
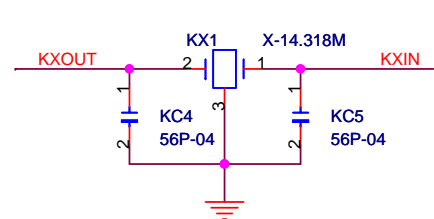
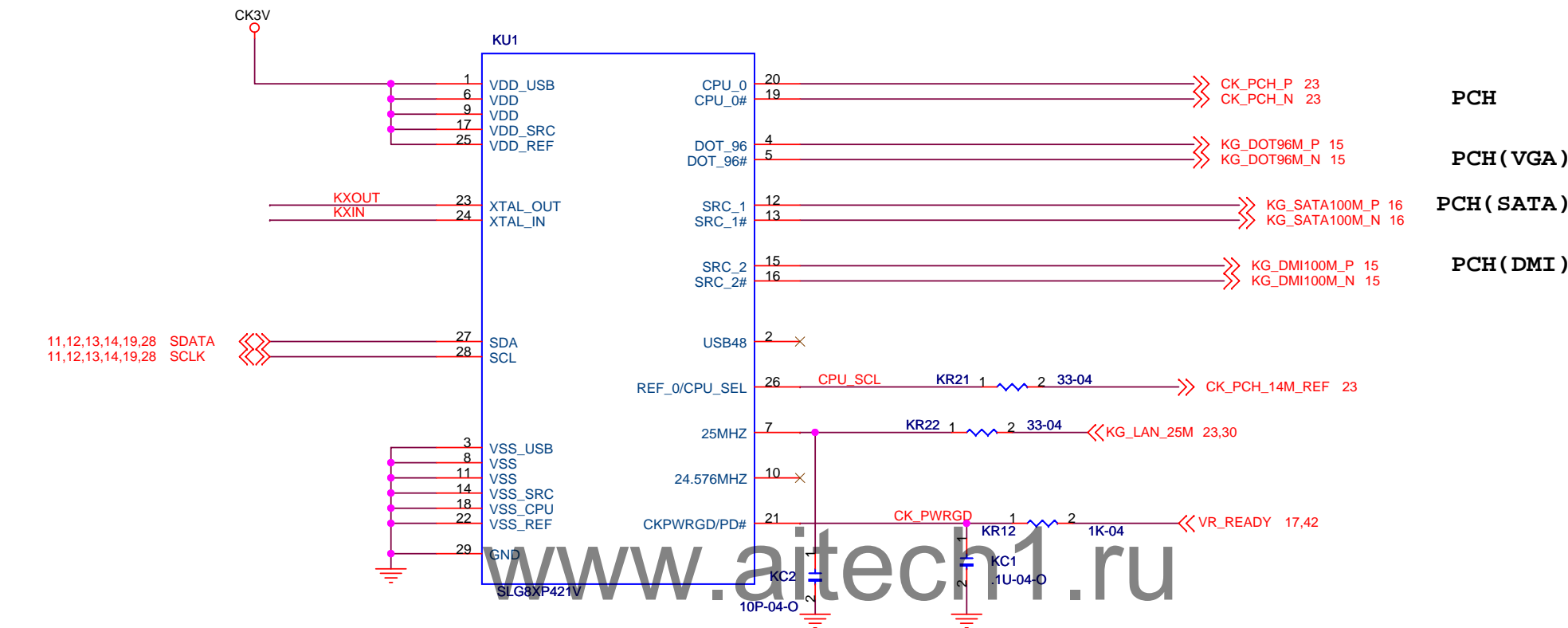
VCORE VCC CPU_VTT	POWER
GND	GND



	Ra	Rb	Ca
NCP5395	Open	0 ohm	Open
NCP5395T	10K	1K	Reserv

PS:NCP5395T is new IC for
PSI transient improvement





0.1uF near the every power pin

PIN 26	CPU_0
0 (default)	133MHz
1 (0.7-1.5V)	100MHz

Elitegroup Computer Systems

Title
SLG8XP421V

Size Custom	Document Number	Rev 1.0
Q57H-AM		

Date: Monday, October 18, 2010
Sheet 43 of 46

ATX P/S WITH 1A STBY CURRENT				
5VSB +/-5%	5V +/-5%	3.3V +/-5%	12V +/-5%	-12V +/-5%

ATX4P1
12V +/-5%

